Code: 13A04701

R13

B.Tech IV Year I Semester (R13) Regular & Supplementary Examinations November/December 2017

**VLSI DESIGN**

(Common to ECE & EIE)

Time: 3 hours

Max. Marks: 70

**PART – A**

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Draw different MOS layers with color codes.
(b) Define Latch-up in a MOS circuit. Mention any one of remedial process to reduce latch-up.
(c) Design a simple NOR gate using CMOS.
(d) Design a CMOS layout by using lambda based rules.
(e) Design a simple EX-NOR gate using CMOS.
(f) Explain about power delay estimation.
(g) Draw the stick diagram for parity generator by using nMOS.
(h) Design a simple logic for memory element.
(i) Discuss about a switch level simulation.
(j) What is controllability in manufacturing test principle?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 Illustrate in detail various processing steps involved in the fabrication of CMOS transistor with necessary diagrams.

**OR**

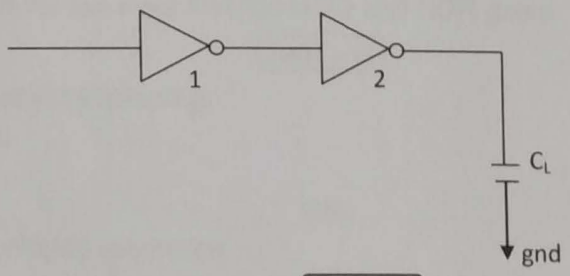
3 Derive the $I_{DS}$ current equation at saturation and non-saturation regions.

**UNIT – II**

4 (a) What is a stick diagram and explain different symbols used for components in stick diagram.
(b) Design a layout diagram for pMOS logic $Y= (AB+CD)^{'}$.

**OR**

5 What is inverter delay? Two nMOS inverters are cascaded to drive a capacitive load $C_L$ = 16 Cg. Calculate the pair delay in turns of $\tau$ for the inverter indicated in the figure below. What are the ratios of each inverter?




**UNIT – III**

6 (a) Explain switch logic and its arrangements
(b) Discuss about the following: (i) Floor-planning. (ii) Placement. (iii) Routing.

**OR**

7 (a) Write a short note on two-phase clocking.
(b) What is placement? Discuss about different levels of placement.

Contd. in page 2

Code: 13A04701

R13

B.Tech IV Year I Semester (R13) Supplementary Examinations June 2017

**VLSI DESIGN**

(Common to ECE & EIE)

Time: 3 hours

Max. Marks: 70

**PART – A**

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) What is Moore's law? State various IC technologies on the basis of number of transistors on a chip.
(b) Define threshold voltage with suitable equation of a MOS device.
(c) What is the figure of merit of a MOS transistor? Mention the suitable expression for figure of merit.
(d) Design a stick diagram for NMOS inverter.
(e) Explain working of pass transistor logic.
(f) Design a two input CMOS NAND gate with neat sketch.
(g) Explain the working of a magnitude comparator.
(h) Compare CPLD and FPGA.
(i) Write a short note on design capture tools.
(j) Explain controllability and observability.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 Explain NMOS fabrication process flow with neat diagrams.

**OR**

3 Draw V-I characteristics of NMOS transistor. Explain its operation. Derive the drain to source current equation in saturation and resistive region.

**UNIT – II**

4 Design a stick and layout diagram for CMOS inverter and two input n-MOS NAND

**OR**

5 (a) Define fan-in and fan-out. Explain their effects on propagation delay.
(b) What do you mean by inverter delay? Explain.

**UNIT – III**

6 What are the alternate gate circuits are available, explain them with suitable sketch?

**OR**

7 Explain about VLSI physical design floor planning.

**UNIT – IV**

8 Implement arithmetic logic unit to perform both arithmetic and logic functions using a full adder.

**OR**

9 Explain the design flow of FPGA.

**UNIT – V**

10 (a) What is meant by synthesis? Explain the circuit synthesis design methods.
(b) What is meant by Simulation? Explain the various VHDL simulations.

**OR**

11 Explain various design capture and verification tools.

*****

Code: 13A04701

R13

B.Tech IV Year I Semester (R13) Regular Examinations November/December 2016

**VLSI DESIGN**

(Common to ECE & EIE)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Distinguish between CMOS and BiCMOS.
(b) Describe the different operating regions for an MOS transistor.
(c) Define Sheet resistance of the MOS device.
(d) What are the limitations of scaling?
(e) Write short notes on switch logic.
(f) What are the different ways to improve clock distribution?
(g) What is parity generator?
(h) What are the advantages and applications of FPGA?
(i) What are the different types of modelling in VHDL?
(j) What is the need for testing?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 Explain clearly about n-well CMOS fabrication process with neat diagrams.

**OR**

3 (a) Draw the V-I characteristics of MOSFET and prove that $I_{ds}$ is linear function of $V_{ds}$.
(b) When the gate to source voltage $V_{GS}$ of a MOSFET with threshold voltage of 400mv, working in saturation is 900mv, the drain current is observed to be 1mA and assuming that the MOSFET is operating at saturation, calculate the drain current for an applied $V_{GS}$ of 1400mv.

**UNIT – II**

4 (a) Define fan-in and fan-out. Explain their effects on propagation delay.
(b) What do you mean by inverter delay? Explain.

**OR**

5 Draw a stick diagram for two input n-MOS NAND and NOR gates.

**UNIT – III**

6 Write short notes about the following:

(a) Pseudo nMOS logic
(b) Domino-Logic

**OR**

7 Discuss about the floor planning.

**UNIT – IV**

8 Explain the working principle of 6-transistor Static RAM and 1-transistor Dynamic RAM with necessary diagrams.

**OR**

9 (a) Draw and explain the architecture of a CPLD.
(b) Differentiate between the Full-custom and Semi-custom design.

**UNIT – V**

10 Explain the design capture and design verification tools.

**OR**

11 Explain the gate level and function level of testing.

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Code: 15A04604 **R15**

B.Tech III Year II Semester (R15) Supplementary Examinations December/January 2018/19

**VLSI DESIGN**

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Differentiate between PMOS and NMOS transistors.
(b) Write the basic DC equations of a MOS transistor design in cutoff, saturation and linear region.
(c) Find the sheet resistance of a material, given the resistivity $\rho = 21\Omega m$ and the thickness is 3m.
(d) Give some limitations of scaling.
(e) Define the terms placement of scaling.
(f) Give comparison of clock routing and power routing.
(g) What is the use of a comparator? Draw the simple comparator circuit?
(h) Differentiate between standard cells and gate arrays.
(i) Define the terms synthesis and simulation.
(j) Why do we need "Design for testability" in a VLSI design?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 Explain in detail about the steps involved in SOI technology fabrication process with essential diagrams.

**OR**

3 Design a CMOS inverter circuit and explain about its various regions of operation in detail with the necessary diagrams.

**UNIT – II**

4 With necessary equations, explain in detail about simple capacitive model and flat band capacitance model.

**OR**

5 (a) Discuss about VLSI design flow.
(b) Write short notes on stick diagram and layout diagram.

**UNIT – III**

6 With a detailed step by step process, design and draw the OR-AND-INVERT form complex gates in CMOS logic for the output expression Y = $\overline{((A+B).(C+D))}$.

**OR**

7 List out the types of routing in a CMOS physical design. And give a detailed note on each one of them.

**UNIT – IV**

8 Draw the truth table for a carry look ahead adder. With the help of K-map reduce the equation and draw the logical circuit diagram for the obtained equation.

**OR**

9 Discuss about design approach of Full custom and Semi-custom devices.

**UNIT – V**

10 Write a short note on the following tools:
(a) Design capture tools.
(b) Design verification tools.

**OR**

11 Explain in detail about Fault modeling and simulation with the necessary example circuits.

*****

Code: 15A04604

R15

B.Tech III Year II Semester (R15) Regular Examinations May/June 2018

**VLSI DESIGN**

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) MOSFETs are said to be more efficient than BJTs. Justify the answer.

(b) Define the terms: (i) Body effect. (ii) Channel length modulation.

(c) How to evaluate routing capacitance of MOS device?

(d) What are the importance of CMOS design rules?

(e) What is the power delay product for the load capacitance $C_L$ = 3.5$\mu F$, given the input voltage $V_{DD}$ = 5 V?

(f) List out the steps in physical design layout.

(g) Mention about various Multiplier architectures followed for VLSI Design.

(h) Give the difference between Full-custom and Semi-custom devices.

(i) What are the special features of design verification tools?

(j) What is Built-in-self-test?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 Explain in detail about the steps involved in CMOS IC fabrication process with essential diagrams.

**OR**

3 Draw the $I_{ds}$-$V_{ds}$ relationship curve and discuss in detail about its role in the MOS design equations.

**UNIT – II**

4 (a) Derive the expression for resistance estimation in VLSI circuits.

(b) Write short notes on driving large capacitive loads.

**OR**

5 (a) Explain the 2$\mu$m CMOS design rules for contacts and transistors.

(b) Briefly discuss about scaling of MOS circuits and its limitations.

**UNIT – III**

6 With a detailed step by step process, design and draw the AND-OR-INVERT form complex gates in CMOS logic for the output equation Y = ($\overline{AB + CD}$).

**OR**

7 Give a detailed note on floor-planning and placement in the physical design flow of a CMOS circuit design.

**UNIT – IV**

8 Explain about any one multiplier architecture in VLSI design. What are the challenging issues to be considered for the same?

**OR**

9 Illustrate with neat architecture diagram and explain about various functional blocks of Field Programmable Gate Array (FPGAs).

**UNIT – V**

10 (a) Write a short note on circuit synthesis.

(b) Give comparison of design capture tools and design verification tools.

**OR**

11 Explain in detail about design for testability.