Code: 15A04802 **R15**

B.Tech IV Year II Semester (R15) Advanced Supplementary Examinations September 2021

LOW POWER VLSI CIRCUITS & SYSTEMS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Define system level measures while designing low power circuits.
(b) What is short channel effect?
(c) Write about the general statement for a standard gate.
(d) Discuss methods of estimating average power in combinational circuits.
(e) What is meant by drain induced barrier lowering?
(f) What are the advantages of dynamic logic circuits?
(g) What is operand isolation?
(h) Explain clock gating with respect to minimizing switched capacitance.
(i) Define glitching power and mention its occurrences.
(j) Why leakage power is an issue? Explain.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Write about different sources of power dissipation.
(b) Explain about sub-threshold leakage in a MOS transistor.

OR

3 (a) Describe the implications of: (i) Power supply voltage. (ii) Threshold voltage. (iii) Scaling on low voltage in low power VLSI design.
(b) Write about drain induced barrier lowering effect in NMOS transistor.

UNIT – II

4 (a) Describe inverter switching characteristics with the help of diagrams.
(b) Discuss about gate logic circuit in detail.

OR

5 (a) Discuss about various MOS inverter delay parameters.
(b) Discuss about single phase and two-phase dynamic circuits and their significance.

UNIT – III

6 (a) Derive an expression for short circuit power dissipation of a CMOS inverter.
(b) What are the limitations of dynamic voltage and frequency scaling? How it is overcome?

OR

7 (a) What are the factors influencing the leakage current in deep sub-micrometer transistor?
(b) List out the advantages of voltage scaling and what is multilevel voltage scaling.

UNIT – IV

8 (a) What is meant by molecule in Transmeta's Crusoe processor?
(b) What is basic assumption of state assignment algorithm?

OR

9 (a) Discuss about hardware software trade-off with an example.
(b) What are the techniques used to reduce power at the logic level?

UNIT – V

10 (a) How are multiple threshold voltages achieved in a circuit? Explain MTCMOS method to reduce leakage power along with its pros and cons.
(b) Discuss about the principles of battery discharge along with battery modeling.

OR

11 (a) Discuss about low power design flow with a diagram.
(b) Differentiate conventional charging with adiabatic charging and explain adiabatic amplification and discuss about realization of adiabatic logic circuits.

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