**Code: 15A04504** **R15**

B.Tech III Year I Semester (R15) Regular Examinations November/December 2017

**DIGITAL SYSTEM DESIGN**

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

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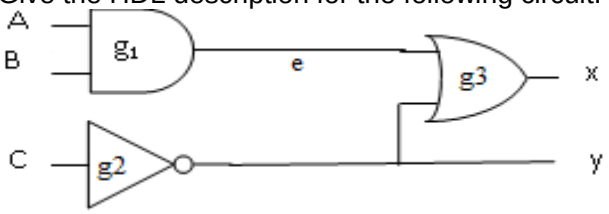
1 Answer the following: (10 X 02 = 20 Marks)

(a) Which is faster TTL or ECL? Which requires more power to operate?

(b) State the characteristics of CMOS family.

(c) Write the HDL data flow description of 4 bit adder.

(d) Give the HDL description for the following circuit.




(e) Why the input variables to a PAL are buffered?

(f) Draw the circuit diagram for 2 to 1 line multiplexer.

(g) How many states are there in a 3 bit ring counter?

(h) Write any two applications of shift register.

(i) Apply gate level model to write a Verilog code for 4-to-2 Encoder.

(j) What is meant by latches?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 With suitable diagrams, explain the interfacing of low voltage CMOS logic with TTL logic family.

**OR**

3 Design a CMOS inverter and explain its operation. Comment on its characteristics such as FAN-in, Fan-out, power dissipation, and propagation delay and noise margin. Compare its advantages over other logic families.

**UNIT – II**

4 (a) Outline the function of test benches of VHDL.

(b) Explain the VHDL features for sequential logic design.

**OR**

5 Enumerate on the structural design elements and behavioral design elements of VHDL with suitable examples.

**UNIT – III**

6 Conclude that the carry look ahead adder is faster than a ripple carry Adder by using necessary equations.

**OR**

7 Implement the following Boolean function using 3 × 4 × 2 PLA, $F_1(x, y, z) = \Sigma (0, 1, 3, 5)$ and $F_2(x, y, z) = \Sigma (3, 5, 7)$.

**UNIT – IV**

8 A sequential machine has one input line where 0's and 1's are being incident. The machine has to produce the output of '1' only when exactly two '0's are followed by '1' or exactly two '1's are followed by a '0'. Using any statement assignment in JK flip flop, synthesize the machine.

**OR**

9 Design and explain the working of 4 bit Johnson counter with neat logic diagram.

**UNIT – V**

10 Develop and test the dual parity encoder by writing VHDL program.

**OR**

11 Analyze the steps involved in the design of shift register using VHDL model.

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**Code: 15A04504**

**R15**

B.Tech III Year I Semester (R15) Supplementary Examinations June 2018

**DIGITAL SYSTEM DESIGN**

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Why commercial ECL families are not as popular as CMOS and TTL?
(b) Define speed-power product. What is its significance?
(c) Write the syntax for VHDL function declaration.
(d) Sketch the VHDL program file structure.
(e) Write the expressions for AGTBOUT and ALTBOUT of a 74x85 comparator.
(f) Interpret 74x999 as a full subtractor.
(g) Define a twisted ring counter.
(h) What is the significance of RCO pin in 74x163 MSI counter?
(i) What is positive and negative triggering in flip-flops?
(j) What is a barrel shifter and how is it different from other shift registers?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 Design logic diagram for AND-OR-INVERT gate. Construct the same using CMOS logic and analyze the circuit with the help of function table.

**OR**

3 Design and summarize the internal 3 sections of LS-TTL NAND gate and analyze the circuit with the help of function table.

**UNIT – II**

4 Model the design flow of VHDL program with front-end and back-end steps.

**OR**

5 Develop a structural VHDL program for a 4-bit prime number detector.

**UNIT – III**

6 Design a 5-to-32 decoder using 74x138's.

**OR**

7 Construct 12-bit comparator using 74x85's and write a VHDL program for comparing 8-bit unsigned integers.

**UNIT – IV**

8 Model the MIS device IC 74x163 in free running mode. Analyze with the help of functional table. Develop VHDL program for a 74x163 like 4-bit binary counter.

**OR**

9 Sketch the logic diagram of 74x194 4-bit universal shift register and develop a VHDL module for the same.

**UNIT – V**

10 Design a 16-bit barrel shifter using 74x151 that performs right circular shift operation. Demonstrate the circuit using VHDL program.

**OR**

11 Design positive edge triggered D flip-flop and explain its functional and timing behaviour. Also develop a VHDL program.

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**Code: 15A04504** **R15**

B.Tech III Year I Semester (R15) Regular & Supplementary Examinations November/December 2018

**DIGITAL SYSTEM DESIGN**

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Define propagation delay.
(b) Which logic family has highest speed of operation?
(c) What is architecture in VHDL?
(d) What are the data types in VHDL?
(e) What is PLA?
(f) What is a combinational PLD?
(g) What is a shift register?
(h) What is Johnson counter?
(i) What is timing verification?
(j) What is fault simulation?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 (a) With a neat circuit diagram, explain the operation of a TTL open collector output.
(b) With a neat circuit diagram, explain the operation of a CMOS open drain and tristate outputs.

**OR**

3 (a) Explain in detail about comparison of different logic families.
(b) Explain IC interfacing for TTL driving CMOS.

**UNIT – II**

4 (a) Explain different delays in VHDL.
(b) Draw the design flow of VHDL and explain each block.

**OR**

5 (a) What are the types of objects in VHDL? Explain each block.
(b) Explain concept of libraries in VHDL.

**UNIT – III**

6 Implement 4-bit ripple adder using 1-bit full adder and write VHDL code for this implementation.

**OR**

7 Explain the operation of comparators and write VHDL code for the corresponding.

**UNIT – IV**

8 Write VHDL code for 4-bit up-down counter with synchronous reset and clear inputs.

**OR**

9 Explain the working of ring counter and write VHDL code for 4-bit ring counter.

**UNIT – V**

10 Explain the difference between D-latch and D-Flip-flop using the process block in VHDL.

**OR**

11 Explain the operation of dual parity encoder and write a VHDL code for the corresponding.

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**Code: 15A04504**

**R15**

B.Tech III Year I Semester (R15) Supplementary Examinations June/July 2019

**DIGITAL SYSTEM DESIGN**

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Draw 2 input NAND gate using basic TTL logic gates.
(b) Define fan-in and fan-out.
(c) Write the syntax of a VHDL entity declaration.
(d) What are unnatural acts in VHDL?
(e) Compare decoder and demultiplexer.
(f) Design a half subtractor.
(g) Convert T Flip Flop to D Flip Flop.
(h) What is the difference between asynchronous and synchronous sequential circuits?
(i) Compare latches and flip-flops.
(j) What is a dual parity encoder?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 Explain in detail low-voltage CMOS logic and interfacing with necessary circuit diagrams.

**OR**

3 Explain with circuit diagram and truth table TTL logic with an example also discuss the logic levels and noise margins of TTL.

**UNIT – II**

4 Discuss the constants and arrays of VHDL.

**OR**

5 Mode a 4 to 1 multiplexer using VHDL behavioral level and selected signal assignment.

**UNIT – III**

6 Implement a full adder circuit with:

(a) Decoder.
(b) Multiplexer.

**OR**

7 Elaborate the concept of PROM, EPROM, EEPROM in detail.

**UNIT – IV**

8 Design a 3-bit bidirectional shift register.

**OR**

9 Explain ring counter with its logic diagram.

**UNIT – V**

10 Discuss the working principle of 4-bit universal shift register.

**OR**

11 Write a VHDL program for a 8-bit comparator.

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**Code: 15A04504** **R15**

B.Tech III Year I Semester (R15) Regular & Supplementary Examinations November/December 2019

**DIGITAL SYSTEM DESIGN**

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Differentiate between the TTL and DTL logic families.
(b) Give the characteristics of TTL logic family.
(c) What is logic synthesis?
(d) What are the behavioural design elements?
(e) Write a VHDL program for 4x1 multiplexer.
(f) Compare PAL and PLA.
(g) Draw the state diagram of modulo-4 up/down counter.
(h) Discuss the steps involved in the analysis of sequential circuits.
(i) List out basic types of programmable logic devices.
(j) Draw the circuit diagram of 3-bit bidirectional shift register.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 (a) List out the advantages and disadvantages of ECL, TTL and CMOS logic family.
(b) Design a 2-input LS-TTL NAND gate and explain its operation. Give the function truth table.

**OR**

3 (a) Design and explain the 2-input OR/NOR gate using ECL logic.
(b) List out the specifications of standards of 74XX and CMOS 40XX series ICs.

**UNIT – II**

4 (a) Explain about the different data types in Verilog HDL.
(b) Define simulation? Explain about gate-level simulation, behavioral simulation and functional simulation.

**OR**

5 (a) Explain the packages and libraries of VHDL.
(b) Explain in detail about post layout timing simulation

**UNIT – III**

6 (a) Design a two-bit comparator circuit and explain its operation.
(b) With neat diagram, explain 3 to 8-line decoder.

**OR**

7 (a) Design a full adder using two half adders. Write VHDL program for the above implementation.
(b) Implement a 2-bit squarer logic circuit using PROM.

Contd. in page 2

**UNIT – IV**

8 (a) Write a VHDL program to design a modulo-8 counter.

(b) Design a 3-bit LFSR counter using 74 × 194. List out the sequence assuming that the initial state is 111.

**OR**

9 (a) Design a self-correcting 4-bit, 4-state ring counter with a single circulating using IC 74LS194.

(b) With a neat sketch, explain the Universal shift register.

**UNIT – V**

10 (a) What is a floating-point encoder? Explain.

(b) Write VHDL code for 4 bit Barrel Shifter.

**OR**

11 (a) What is a PLD? Compare the three combinational PLDs?

(b) Discuss the logic circuit of 74 × 377 register. Write a VHDL program for the same in structural style.

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**Code: 15A04504** **R15**

B.Tech III Year I Semester (R15) Supplementary Examinations October 2020

**DIGITAL SYSTEM DESIGN**

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Describe the key benefit of Schottky transistors in TTL.
(b) What are the disadvantages of ECL gates?
(c) Write the syntax for package.
(d) Discuss about technology libraries.
(e) Write a VHDL program for 2 x 4 Decoder.
(f) How full adder is different from full subtractor? Explain.
(g) Write modes of operation of shift registers.
(h) Write a VHDL code for 3-bit ring counter.
(i) Explain about parallel in serial out shift register.
(j) What are the applications of flip flops?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 (a) How to interface CMOS with TTL logic. Give its constraints.
(b) Draw the circuit diagram of basic TTL NAND gate and explain with the help of functional operation.

**OR**

3 (a) What are the salient features of ECL? And explain its internal structure.
(b) Compare various types of logic families.

**UNIT – II**

4 (a) Explain about the following: (i) Concurrency. (ii) Simulation. (iii) Synthesis. (iv) System tasks.
(b) Explain about the data types, scalar and vector parameters, keywords in VHDL.

**OR**

5 (a) Explain various primitives available in VHDL and give one example for one of the primitive.
(b) Explain about compiler directives.

**UNIT – III**

6 (a) What is the function of magnitude comparator? Explain with an example.
(b) Design a priority encoder for 16 inputs using two 74 × 148 encoders.

**OR**

7 (a) Implement a full-adder circuit with a decoder and two OR gates.
(b) Compare PROM, PAL and PLA.

**UNIT – IV**

8 (a) Design an 8-bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.
(b) Explain in detail about the working of Johnson Counter using 74 LS194.

**OR**

9 (a) Define state, state diagram. Draw state diagram taking any one as an example.
(b) Design MOD-16 synchronous counter using T- Flip-Flop.

**UNIT – V**

10 (a) Draw the block diagram and explain in detail about the PAL.
(b) Write Verilog module for 8-bit comparator with test bench.

**OR**

11 (a) Design a 3-bit synchronous up counter using T Flip-flops.
(b) Explain the design of a 4-bit binary counter with parallel load in detail.

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