JNTUA UNIVERSITY
PREVIOUS QUESTION PAPERS

Code: 13A04701 **R13**

B.Tech IV Year I Semester (R13) Supplementary Examinations June 2017

VLSI DESIGN

(Common to ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What is Moore's law? State various IC technologies on the basis of number of transistors on a chip.
(b) Define threshold voltage with suitable equation of a MOS device.
(c) What is the figure of merit of a MOS transistor? Mention the suitable expression for figure of merit.
(d) Design a stick diagram for NMOS inverter.
(e) Explain working of pass transistor logic.
(f) Design a two input CMOS NAND gate with neat sketch.
(g) Explain the working of a magnitude comparator.
(h) Compare CPLD and FPGA.
(i) Write a short note on design capture tools.
(j) Explain controllability and observability.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain NMOS fabrication process flow with neat diagrams.

OR

3 Draw V-I characteristics of NMOS transistor. Explain its operation. Derive the drain to source current equation in saturation and resistive region.

UNIT – II

4 Design a stick and layout diagram for CMOS inverter and two input n-MOS NAND

OR

5 (a) Define fan-in and fan-out. Explain their effects on propagation delay.
(b) What do you mean by inverter delay? Explain.

UNIT – III

6 What are the alternate gate circuits are available, explain them with suitable sketch?

OR

7 Explain about VLSI physical design floor planning.

UNIT – IV

8 Implement arithmetic logic unit to perform both arithmetic and logic functions using a full adder.

OR

9 Explain the design flow of FPGA.

UNIT – V

10 (a) What is meant by synthesis? Explain the circuit synthesis design methods.
(b) What is meant by Simulation? Explain the various VHDL simulations.

OR

11 Explain various design capture and verification tools.

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PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) What is Moore's law? State various IC technologies on the basis of number of transistors on a chip.
(b) Describe the different operating regions for an MOS transistor.
(c) What is figure of merit of a MOS transistor? Mention suitable expressions for figure of merit.
(d) What are the limitations of scaling?
(e) Explain working of pass transistor logic.
(f) What are the different ways to improve clock distribution?
(g) Explain working of magnitude comparator.
(h) What are the advantages and applications of FPGA?
(i) What are the different types of modeling in VHDL?
(j) Explain controllability and observability.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain clearly about NMOS fabrication process flow with neat diagrams.

OR

3 Draw the V-I characteristics of MOSFET and prove that I_{ds} is linear function of V_{ds}.
When the gate to source voltage V_{GS} of a MOSFET with threshold voltage of 400 mv, working in saturation is 900 mv, the drain current is observed to be 1 mA and assuming that the MOSFET is operating at saturation, calculate the drain current for an applied V_{GS} of 1400 mv.

UNIT – II

4 (a) Define fan-in and fan-out. Explain their effects on propagation delay.
(b) What do you mean by inverter delay? Explain.

OR

5 Design a stick and layout diagram for CMOS inverter and two inputs NMOS NAND gate.

UNIT – III

6 What are the alternate gate circuits are available? Explain them with suitable sketch.

OR

7 Discuss about the floor planning.

UNIT – IV

8 Explain the working principle of 6-transistor static RAM and 1-transistor dynamic RAM with necessary diagrams.

OR

9 Explain in detail about design flow of FPGA.

UNIT – V

10 Explain the design capture and design verification tools.

OR

11 What is meant by synthesis? Explain the circuit synthesis design methods.

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Code: 15A04604 **R15**

B.Tech III Year II Semester (R15) Regular Examinations May/June 2018

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) MOSFETs are said to be more efficient than BJTs. Justify the answer.

(b) Define the terms: (i) Body effect. (ii) Channel length modulation.

(c) How to evaluate routing capacitance of MOS device?

(d) What are the importances of CMOS design rules?

(e) What is the power delay product for the load capacitance $C_L = 3.5\mu F$, given the input voltage $V_{DD} = 5$ V?

(f) List out the steps in physical design layout.

(g) Mention about various Multiplier architectures followed for VLSI Design.

(h) Give the difference between Full-custom and Semi-custom devices.

(i) What are the special features of design verification tools?

(j) What is Built-in-self-test?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain in detail about the steps involved in CMOS IC fabrication process with essential diagrams.

OR

3 Draw the I_{ds}-V_{ds} relationship curve and discuss in detail about its role in the MOS design equations.

UNIT – II

4 (a) Derive the expression for resistance estimation in VLSI circuits.

(b) Write short notes on driving large capacitive loads.

OR

5 (a) Explain the 2μm CMOS design rules for contacts and transistors.

(b) Briefly discuss about scaling of MOS circuits and its limitations

UNIT – III

6 With a detailed step by step process, design and draw the AND-OR-INVERT form complex gates in CMOS logic for the output equation $Y = \overline{(AB + CD)}$

OR

7 Give a detailed note on floor-planning and placement in the physical design flow of a CMOS circuit design.

UNIT – IV

8 Explain about any one multiplier architecture in VLSI design. What are the challenging issues to be considered for the same?

OR

9 Illustrate with neat architecture diagram and explain about various functional blocks of Field Programmable Gate Array (FPGAs).

UNIT – V

10 (a) Write a short note on circuit synthesis.

(b) Give comparison of design capture tools and design verification tools.

OR

11 Explain in detail about design for testability.

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