JNTUA UNIVERSITY
PREVIOUS QUESTION PAPERS

Code No: R09220204 R09 **SET-1**

B.Tech II Year - II Semester Examinations, April-May, 2012

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, ETM, BME)

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

1.a) Convert the number (17.125)16 to base 10, base 4, base 5 and base 2.

b) Perform the binary arithmetic operations on (-14)-(-2) using signed 2's complement representation.

c) Justify the statement that "Gray code is a class of reflected code". [6+6+3]

2.a) State and Prove De Morgan's theorem of Boolean Algebra.

b) Determine the canonical product-of-sums and sum-of-products form of T(x,y,z) = x'(y' + z')

c) Realize the basic gates using NAND and NOR gates only. [5+ 4+6]

3.a) Prove that if w'x + yz' = 0, then wx + y'(w' + z') = wx + xz + x'z' + w'y'z.

b) For the given function T(w,x,y,z) = Σ (0,1,2,3,4,6,7,8,9,11,15)

i) Show the map

ii) Find all prime implicants and indicate which are essential.

iii) Find a minimal expression for T and realize using basic gates. Is it unique? [7+8]

4.a) Design a 2-bit comparator which compares the magnitude of two numbers X and Y and generates three output f1,f2, and f3.

b) Realize 16 × 1 Mux using only 2 × 1 Mux. [8+7]

5.a) Realize the given function using PLD circui F(x,y,z) = xy + yz + x'y' .

b) What is meant by Logic simulation, Functional simulation, timing simulation and Logic synthesis? [9+6]

6.a) Design a BCD counter using JK Flip-Flops.

b) Write the differences between synchronous and asynchronous counters.

c) Draw the state diagram and characteristic table of Master Slave JK flip-flop. [8+3+4]

7.a) Write the differences between completely specified function and incompletely specified functions with examples.

b) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 0, input X is transferred to Z, otherwise, the output remains same. [6+9]

8.a) Differentiate between Mealy and Moore machine with examples.

b) Write about the implementation of Binary multiplier. [8+7]

Code No: R09220204 R09 **SET-2**

B.Tech II Year - II Semester Examinations, April-May, 2012

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, ETM, BME)

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

1.a) Convert the number (127.75)8 to base 10, base 3, base 16 and base 2.

b) Given that (64)10 = (100)b , determine the value of b.

c) Perform the binary arithmetic operations on (+12)-(4) using signed 2'scomplement representation. [5+4+6]

2.a) State and Prove the Huntington postulates of Boolean Algebra.

b) Find the complement of the function and represent in sum of minterms F(x,y,z) = xy + z'

c) Simplify the following function and realize using universal gates F(A,B,C) = A'BC' + ABC + B'C' + A'B' [5+4+6]

3.a) Use the tabulation procedure to generate the set of prime implicants and to obtain all minimal expressions for the following function F(a,b,c,d) = Σ (1,5,6,12,13,14) + Σd(2,4)

b) For the given function T(w,x,y,z) = Σ (0,1,5,7,8,10,14,15)

i) Show the map

ii) Find all prime implicants and indicate which are essential.

iii) Find a minimal expression and realize using basic gates. [8+7]

4.a) Design a combinational circuit to find the 2's complement of a given 4bit binary number and realize using NAND gates.

b) Design a full adder using Multiplexer. [8+7]

5.a) What is PAL? How does it differ from PROM and PLA?

b) Design a switching circuit that converts a 4 bit binary code into a 4 bit Gray code using ROM array. [6+9]

6.a) Define Setup and Hold times.

b) Write the characteristic, excitation tables for JK, RS, T and D flip-flops.

c) Design a synchronous counter to generate the sequence 0,1,1,2,3,5,8, and repeat the sequence using T flip-flops. [2+6+7]

7.a) Construct the state diagram and primitive flow table for an asynchronous Machine that has two inputs and one output. The input sequence xy = 00, 01, 10 Causes the output to become 1. The next input change then causes the output to return to 0. No other inputs will produce a 1 output.

b) Write the usage of merger graph with example. [8+7]

8.a) Write the usage of Mealy machine with example.

b) Discuss the implementation of Binary multiplier with appropriate realizations. [8+7]

Code No: R09220204 R09 **SET-3**

B.Tech II Year - II Semester Examinations, April-May, 2012

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, ETM, BME)

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

1.a) Convert the following to the required form.

i) (A98B)12 = (---------)3 ii) (38.65)10 = (-----------)2.

b) Use 2's complement form perform subtraction.

i) 1101010-110100 ii) 10011.1101-101.11 [15]

2.a) Simplify the following

i) (A+ AC + B) ii) F = AB(C +C) + AB iii) F = (X +Y)(X + Z)

b) Prove that NAND and NOR gates are Universal gates. [15]

3.a) Simplify the following function using K-map.

F(A,B,C,D) = Σ(1,3,4,5,6,11,13,14,15)

b) Simplify the following using Tabular method.

F(A,B,C,D) = Σ(3,7,8,12,13,15)+ (9,14) φ Σ . [15]

4.a) Design a 64:1 MUX using 8:1 MUXs.

b) Design a 4 bit parallel adder using Full adder modules. [15]

5.a) Design a 4-bit parity checker/ generator circuit that can generate even parity using logic gates.

b) Write a brief note on threshold logic synthesis. [15]

6.a) What is meant by clock skew? How to handle it?

b) Explain the term Race around condition. How is it satisfied by Master-slave Flip-Flops. [15]

7.a) Design a modulo 10 counter JK flipflops.

b) What are the rules to develop a Merger chart? [15]

8. Design a binary multiplier and its control logic by drawing ASM chart and realize the same using decoder, MUX and D flipflops. [15]

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Code No: R09220204 R09 **SET-4**

B.Tech II Year - II Semester Examinations, April-May, 2012

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, ETM, BME)

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

1.a) Develop a Gray code for (42)10 and (97)10 and convert the same to Hex sequence.

b) Explain different error detecting and correcting codes in digital system. [15]

2.a) Show that i) AB + AB = A Å B

ii) (A Å B) = (A e B)

b) Reduce the following boolean expressions using theorems and identities.

i) F = C + AB + AD(B + C)+ CD

ii) F = AB + CDB + ACD [15]

3.a) Simplify the following using prime implicant chart method.

f(A,B,C,D) = Σ(0,5,7,8,9,10,11,13)

b) Use tabular method and simplify the following 5 variable function

F(A,B,C,D,E) = Σ(0,4,8,12,16,20,24,28) + Σϕ (1,5,7,23). [15]

4.a) Design a 4 bit comparator circuit using logic gates.

b) Design a code converter logic circuit which converts BCD code to Excess-3 code. [15]

5.a) Design a square generator logic for 4 bit input using ROM.

b) What are the capabilities and limitations of threshold gate? [15]

6.a) Convert RS flip flop to a

i) D-latch ii) T-latch.

b) Design a FSM which detects 0011 pattern and set z = 1 for all other patterns z = 0 [15]

7.a) Design a multi mode universal shift registers of 4 bit.

b) Draw a block diagram of Modulo 10 ripple counter and explain its timing diagram. [15]

8. Design a control logic through ASM Chart for the sequence detector which detects 1100 and resets flip flop F to 0 and flip flop E to 1. The patterns come from 4 bit counter A. [15]

Code: 13A04303 **R13**

B.Tech II Year I Semester (R13) Supplementary Examinations November/December 2016

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What is the decimal equivalent of hexadecimal number 1A53?

(b) Simplify the following Boolean expression: (A'BC')'+ (AB'C)'.

(c) Simplify the following function using K- map: F(x, y, z) = Σ(2, 3, 4, 5).

(d) Construct a logic circuit using NAND gates only for the expression x = A.(B + C).

(e) What do you understand by Combinational logic circuits? Give example.

(f) What is multiplexer? Draw the block diagram of 4-input MUX.

(g) What is the difference between latch and flip flop?

(h) What is shift register? List out some applications of Shift Register.

(i) How race around condition can be eliminated?

(j) What are hazards in digital logic circuits? How they can be resolved?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Simplify the following identities using Boolean algebra:

(a) (A+B)(A+(AB')')C+A'(B+C')+A'B+ABC.

(b) $\overline{A\overline{(A \cdot B)} \cdot B\overline{(A \cdot B)}}$

OR

3 (a) Simplify and draw the logic diagram for the given expression:
F = (ABC)'+ (AB)'C+ A'BC'+ A(BC)'+ AB'C

(b) Simplify the expressions using Boolean postulates: F= XY + (XZ)'+ XY'Z (XY + Z).

UNIT – II

4 (a) Simplify the following expression using the K-map: Y = A'B'C'+ AC'D' + AB'+ ABCD' + A'B'C

(b) Write the expression for Boolean function F (A, B, C) = ∑m (1, 4, 5, 6, 7) in standard POS form.

OR

5 Simplify the following expression to sum of products using Tabulation Method:
F(a, b, c, d)=∑m(0,4,8,10,12,13,15) +d(1,2)

UNIT – III

6 Discuss in detail, the working of full adder logic circuit and extend your discussion to explain a binary adder, which can be used to add two binary numbers.

OR

7 (a) Draw the logic circuit of a 3 to 8 decoder and explain its working.

(b) Explain the working of a De-multiplexer with the help of an example.

UNIT – IV

8 Using D-Flip flops and waveforms, explain the working of a 4-bit SISO shift register.

OR

9 With the help of clocked JK flip flops and waveforms, explain the working of a 3-bit binary ripple counter. Write truth table for clock transitions.

UNIT – V

10 Difference between static and dynamic RAM. Draw the circuits of one cell of each and explain its working.

OR

11 Is the ROM a volatile memory? Explain. Also draw the logic diagram of 16-bit ROM Array and explain its principle of operation.

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Code: 13A04303

R13/SS

B.Tech II Year II Semester (R13) Supplementary Examinations December/January 2015/2016

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE and ECE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) State and Prove consensus theorem.
(b) Find the 2's complement of representation of -9.
(c) Design a XOR gate using minimum number of NAND gates.
(d) Find the minimum number of literals for the following function using 2 variable Karnaugh Map.
F = =∑m (1) + d (3). d - Don't care.
(e) Write the sum and carry expression for half adder.
(f) Implement the function F =∑m (0, 2) using a 2 × 4 decoder.
(g) Write the characteristic equation for JK Flip-flop.
(h) How many states are there in a n-bit ring counter?
(i) Compare PROM & PAL.
(j) What is meant by cycle in asynchronous circuits?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Express the following function F = xy + x' y in a product of max-terms.
(b) Check if NOR gate is associative or not.

OR

3 (a) Show that a positive logic NAND gate is a negative logic OR gate
(b) Obtain the truth table of the following function and express in sum of min-terms and product of max-terms: F = (A' + B).(B' + C).

UNIT – II

4 Simplify the Boolean function using K map technique:

(a) F = π M (3, 4, 6, 7, 11, 12, 13, 14, 15).
(b) F = ∑m (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14).

OR

5 Simplify the following Boolean function using tabulation method:
F = ∑m (0, 1, 2, 3, 5, 7, 8, 10, 14, 15).

UNIT – III

6 Design a 4-Bit Magnitude comparator using logic gates.

OR

7 (a) Implement the function F = ∑m (0, 1, 2, 4, 5, 8, 11, 12, 15) using 8:1 multiplexer.
(b) Design a half subtractor using logic gates.

UNIT – IV

8 Design a 4 bit universal shift register with neat diagram.

OR

9 Design a 3 bit synchronous up counter using T Flip-flops.

UNIT – V

10 Implement the following functions using PLA with three inputs, four product terms and two outputs.
F1 (A, B, C) = ∑m (3, 5, 6, 7), F2 (A, B, C) = ∑m (0, 2, 4, 7).

OR

11 Implement the switching function F = ∑m (1, 3, 5, 7, 8, 9, 14, 15) by a static hazard free two level AND-OR network.

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Code: 13A04303 **R13**

B.Tech II Year I Semester (R13) Regular & Supplementary Examinations December 2015

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) State and prove De-Morgans theorem.
(b) What do you understand by universal gate?
(c) Convert the given equation Y=AB+AC'+BC into standard SOP form.
(d) Implement the following Boolean equation using only NAND gates Y=AB+CDE+F.
(e) Draw the logic diagram of full adder circuit and form the truth table.
(f) What is multiplier? Draw the block diagram of 4-input MUX.
(g) Give the comparison between combinational circuits and sequential circuits.
(h) What is shift register? Give the classification of them.
(i) What are the steps involved in designing an asynchronous sequential circuits?
(j) What are hazards in digital logic circuits? How it can be resolved?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Simplify the following Boolean expression: (i) F = (A+B)(A'+C)(B+C). (ii) F = A+B+C'+D(E+F)'

OR

3 (a) Expand the following Boolean functions F = xy+x'zin a standard product of maxterm form.
(b) Minimize the following Boolean function: $f(A,B,C,D)=\sum m(5,7,8,10,13,15)+\sum d(0,1,2,3)$.

UNIT – II

4 (a) Simplify the following expression using the K-map for the 4-variable:
Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C'
(b) Implement the following Boolean function using NOR gates Y=(AB'+A'B)(C+D').

OR

5 Simplify the Boolean function by using tabulation method.
$F(a,b,c,d)=\sum m(0,1,2,5,6,7,8,9,10,14)$

UNIT – III

6 Discuss in detail about the design procedure for binary serial and parallel adder with diagram.

OR

7 Implement a 2-bit Magnitude comparator and write down its design procedure.

UNIT – IV

8 A sequential circuit with two D-flip flops A and B, two inputs 'x' and 'y' and one output 'z' is specified by the following next state and output equation.
A(t+1) = x'y+xA, B(t+1) = x'B+xA and Z = B
(i) Draw the logic diagram of the circuit. (ii) List the state table and draw the corresponding state diagram.

OR

9 Design and implement 3-bit ripple counter using J-K flip flop. Draw the state diagram, logic diagram and timing diagram for the same.

UNIT – V

10 What is critical and non-critical races in asynchronous circuits? How to avoid races? Illustrate with one example.

OR

11 Design and implement the following Boolean functions in PAL.

(a) $A(w,x,y,z)=\sum m(0,2,6,7,8,9,12,13)$
(b) $B(w,x,y,z)=\sum m(0,2,6,7,8,9,12,13,14)$
(c) $C(w,x,y,z)=\sum m(1,3,4,6,10,12,13)$
(d) $D(w,x,y,z)=\sum m(1,3,4,6,9,12,14)$

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Code: 13A04303 R13

B.Tech II Year I Semester (R13) Supplementary Examinations June 2015

SWITCHING THEORY AND LOGIC DESIGN

(Common to ECE & EIE)

Time: 3 hours Max. Marks: 70

PART - A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Find the complement of the function $F = A + BC$ and show that $F.\overline{F} = 0$.

(b) Perform the subtraction operation on 22-7 using 2's complement form.

(c) Convert the expression $f(A,B,C) = (A+B)(B+C)(A+C)$ in standard POS form.

(d) Simplify $\overline{\overline{A}B + \overline{A} + AB}$.

(e) Obtain the prime implicates for given Boolean expression. $f(A,B,C) = \sum(0,1,3,5,7)$ using k-map.

(f) Design a 4 bit parallel adder using Full adders.

(g) Explain how decoder can be converted into a demultiplexer with a neat block diagram.

(h) Compare PROM, PLA & PAL.

(i) Compare level and edge triggering.

(j) Assume that the 5 bit binary counter starts in the 0000 state then what will be the count after 144 input pulses.

PART - B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT - I

2 Encode the decimal number 365 in
(i) Binary (ii) BCD (iii) ASCII (iv) Excess – 3.

OR

3 Given the 8 – bit data word 01011011 generate the 12 bit composite word for the hamming code that corrects and detects single errors.

UNIT - II

4 (a) Implement the Boolean expression for Ex-OR gate using NAND gates.

(b) Simplify the Boolean expression $\overline{A}B\left(\overline{D} + \overline{C}D\right) + B(A + \overline{A}CD)$ to one literal.

OR

5 (a) Implement Ex- NOR gate using only NOR gates.

(b) Use the K-map method to simplify the following 5-variable function
$F = \sum(3,6,7,8,10,12,14,17,19,20,21,24,25,27,31)$

UNIT - III

6 (a) What is a decoder? Construct 3×8 decoder using logic gates and also write truth table.

(b) Design a 4 bit odd parity generator. Mentions its truth table.

OR

7 (a) Implement the following Boolean function using 8:1 multiplexer.
$F(A,B,C,D) = \overline{A}B\,\overline{D} + ACD + \overline{B}CD + \overline{A}\,\overline{C}D$

(b) Design a 2 bit comparator using gates.

UNIT - IV

8 (a) Construct a JK flip-flop using D flip-flop, 2×1 multiplexer and an inverter.

(b) Convert SR flip – flop to T flip – flop.

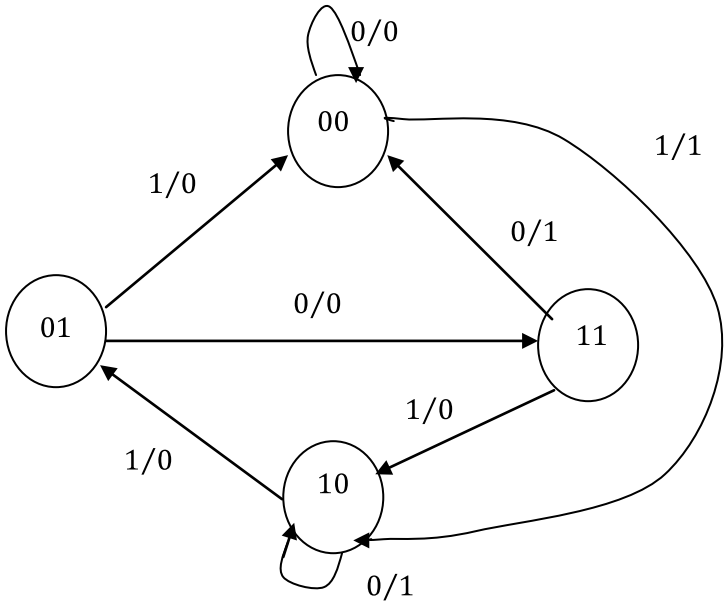
OR

9 Define the following terms in connection with a flip-flop
(i) Setup time (ii) Hold time (iii) Propagation delay time (iv) Preset (v) Clear.

Contd. in page 2

UNIT – V

10 A sequential circuit has one input and one output. The state diagram is shown below:



Design the sequential circuit with (a) D flip-flop (b) RS flip-flop (c) JK flip-flop.

OR

11 (a) Implement the following Boolean function using PLA

$F_1(w.x.y.z) = \sum(0,1,3,5,9,13)$

$F_2(w,x,y,z) = \sum(0,2,4,5,7,9,11,15)$

(b) What is hazard in switching circuits? Explain the design of hazard free switching circuit with an example.

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Code: 13A04303

R13

B.Tech II Year I Semester (R13) Regular Examinations December 2014

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) If $143_5 = X_6$, then X is…..

(b) Minimum number of two input NAND gates required to implement Y = A + B C.

(c) What is the importance of don't care conditions?

(d) SOP of F(x, y, z)=∑(2, 3, 6, 7).

(e) Implement OR gate using only two input NAND gates?

(f) Draw the block diagram of 2x4 decoder with enable.

(g) Draw the block diagram of sequential circuit using combinational circuit and memory unit.

(h) Draw the logic circuit of flip-flop and truth table using NOR gates.

(i) What is the function of EAROM?

(j) Mention few applications of PLA.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Convert the following to Decimal and then to Octal. (i) 4234_{16} (ii) 10010011_2

(b) Implement the function with NOR-NOR logic Y= A C + B C + A B+ D.

OR

3 (a) Convert the following to Decimal and then to Hexadecimal. (i) 1234_8 (ii) 11001111_2

(b) Find the complement of the following Boolean function and reduce into minimum number of literals.
Y= BC'+A'D)(DB'+CD'

UNIT – II

4 Simplify the following Boolean expressions using K-map and implement them using NAND gates.
F(W,X,Y,Z)= XZ+W'XY'+WXY+W'YZ+WY'Z

OR

5 Simplifying the following expression using tabulation technique.
F=∑m(0,1,2,8,9,15,17,21,24,25,27,31)

UNIT – III

6 (a) Design a 4 bit binary-to-Gray code converter.

(b) Realize a 2-bit comparator.

OR

7 (a) Design a 4 bit binary-to-BCD code converter.

(b) Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux.

UNIT – IV

8 (a) Draw the circuit of JK flip flop using NAND gates and explain its operation.

(b) Design a 2-input 2-output detector which produces an output 1 every time the sequence 0101 is detected. Implement the sequence detector using JK flip-flops.

OR

9 (a) Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram.

(b) A clocked sequential circuit with single input x and single output z produces an output z=1 whenever the input x compares the sequence 1011 and overlapping is allowed. Obtain the state diagram, state table and design the circuit with D flip-flops.

UNIT – V

10 (a) Explain about ROM and PROM.

(b) Design a BCD to excess-3 code converter using ROM.

OR

11 (a) What is Race-free state Assignment? Explain.

(b) Realize f=∑m(0,2,3,7,9,11,15,16) using ROM.

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Code: 13A04303 **R13/SS**

B.Tech II Year II Semester (R13) Supplementary Examinations May/June 2019

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE and ECE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Find the 10's compliment of the decimal value 012398_{10}.

(b) Find the complement of the function $F_1 = x(y'z' + yz)$ by applying DeMorgan's theorem as many times as necessary.

(c) Simplify the Boolean function $F(x, y, z) = \sum(0,1,5,7)$ using three-variable map.

(d) Draw the logic diagram of a 3-bit even parity generator.

(e) Given X-OR gate has a propagation delay of 20 ns and AND or OR gates have a propagation delay of 10 ns. Find the total propagation delay in a full adder.

(f) Give the steps involved in designing a combinational circuit.

(g) Define trigger in a flip-flop.

(h) List out the applications of shift registers and counters,

(i) An asynchronous sequential circuit is described by excitation function $Y = x_1x_2' + (x_1 + x_2')y$. Draw the logic diagram of the circuit.

(j) Differentiate between RAM and ROM.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Simplify and draw the logic diagram for the given expression:

$A = (ABC)' + (AB)'C + A'BC' + A(BC)' + AB'C$

(b) Simplify the following identities using Boolean algebra:

$(A + B)(A + (AB)')C + A'(B + C') + A'B + ABC$

OR

3 (a) State and prove DeMorgan's law of union.

(b) Express the Boolean function $F = xy + x'z$ in a product of maxterm form.

UNIT – II

4 (a) Simplify the Boolean function $F(w, x, y, z) = \sum(2,3,10,11,12,13,14,15)$ using four-variable K-map.

(b) Simplify the Boolean function $(A' + B' + D')(A + B' + C')(A' + B + D')(B + C' + D')$ in sum of product.

OR

5 (a) Implement the Boolean function $F = xy' + x'y' + z$ by using NAND gates.

(b) By using tabulation methods simplify the function:

$Z = f(A, B, C) = A'B'C' + A'B'C + AB'C' + AB'C$

UNIT – III

6 Derive the expression for BCD to excess-3 code converter using K-map and implement the combinational logic circuit of it.

OR

7 Implement the following functions using a multiplexer:

(i) $F(x, y, z) = \sum(1,2,6,7)$

(ii) $F(A, B, C, D) = \sum(1,3,4,11,12,13,14,15)$

Contd. in page 2

UNIT – IV

8 Reduce the number of states in the following state table and tabulate the reduced state table shown below:

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

OR

9 With a neat circuit diagram and function table, explain the logical operation of a 4-bit universal shift register in detail.

UNIT – V

10 Explain in detail about the design procedures involved with designing an asynchronous sequential circuit by minimizing the circuit complexity and producing a stable circuit without critical races.

OR

11 (a) Draw the timing waveforms for read and write memory cycle in a Random Access Memory.

(b) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number.

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Code: 13A04303

R13/SS

B.Tech II Year II Semester (R13) Supplementary Examinations December/January 2015/2016

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE and ECE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) State and Prove consensus theorem.
(b) Find the 2's complement of representation of -9.
(c) Design a XOR gate using minimum number of NAND gates.
(d) Find the minimum number of literals for the following function using 2 variable Karnaugh Map.
F = =∑m (1) + d (3). d - Don't care.
(e) Write the sum and carry expression for half adder.
(f) Implement the function F =∑m (0, 2) using a 2 × 4 decoder.
(g) Write the characteristic equation for JK Flip-flop.
(h) How many states are there in a n-bit ring counter?
(i) Compare PROM & PAL.
(j) What is meant by cycle in asynchronous circuits?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Express the following function F = xy + x' y in a product of max-terms.
(b) Check if NOR gate is associative or not.

OR

3 (a) Show that a positive logic NAND gate is a negative logic OR gate
(b) Obtain the truth table of the following function and express in sum of min-terms and product of max-terms: F = (A' + B).(B' + C).

UNIT – II

4 Simplify the Boolean function using K map technique:

(a) F = π M (3, 4, 6, 7, 11, 12, 13, 14, 15).
(b) F = ∑m (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14).

OR

5 Simplify the following Boolean function using tabulation method:
F = ∑m (0, 1, 2, 3, 5, 7, 8, 10, 14, 15).

UNIT – III

6 Design a 4-Bit Magnitude comparator using logic gates.

OR

7 (a) Implement the function F = ∑m (0, 1, 2, 4, 5, 8, 11, 12, 15) using 8:1 multiplexer.
(b) Design a half subtractor using logic gates.

UNIT – IV

8 Design a 4 bit universal shift register with neat diagram.

OR

9 Design a 3 bit synchronous up counter using T Flip-flops.

UNIT – V

10 Implement the following functions using PLA with three inputs, four product terms and two outputs.
F1 (A, B, C) = ∑m (3, 5, 6, 7), F2 (A, B, C) = ∑m (0, 2, 4, 7).

OR

11 Implement the switching function F = ∑m (1, 3, 5, 7, 8, 9, 14, 15) by a static hazard free two level AND-OR network.

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Code: 13A04303

R13

B.Tech II Year I Semester (R13) Supplementary Examinations November/December 2018

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Draw the symbol of universal gates.
(b) State the Demorgan's theorem.
(c) Expand POS and SOP.
(d) Realize AND operation by using NAND gates.
(e) Define decoder.
(f) Mention two applications multiplexer.
(g) What is the drawback of SR latch?
(h) Define counter.
(i) List out the types of PLDs.
(j) Define hazards in logic design.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Perform subtraction by using 10's complement for the given 845-245.
(b) Perform subtraction by using 2's complement for the given 111011-1010.

OR

3 Interpret the following to decimal and then to binary:
(i) 10111_6. (ii) $ABCD_{16}$. (iii) 7234_8. (iv) 1100_2.

UNIT – II

4 Minimize using K-map and realize by NAND gates F(A,B,C,D) = Σ(0,1,2,3,12,13,14,15).

OR

5 (a) Minimize and realize, $F = \overline{(\bar{X} + \bar{Y} + Z)} + Z + WZ$ by basic gates.
(b) Realize Ex-OR and Ex-NOR gate operations by NOR gates.

UNIT – III

6 Construct BCD adder and explain the operation.

OR

7 (a) Implement F=Σ(0,1,2,3) using decoder,
(b) Design 3X3 binary multiplier.

UNIT – IV

8 (a) Develop 3 bit ripple up counter.
(b) Create the circuit of JK flip-flop using NAND gates and explain its operation.

OR

9 (a) Derive the characteristics table and characteristic equation of DFF.
(b) Design T flip flop by using SR flip flop.

UNIT – V

10 (a) Write the differences between PAL and PLA.
(b) Minimize and implement the Boolean function F = Σ(0,1,2,3,13,14,15) using PROM.

OR

11 Explain about analysis procedure in sequential circuits in detail.

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