JNTUA UNIVERSITY
PREVIOUS QUESTION PAPERS

Code: 13A04804 **R13**

B.Tech IV Year II Semester (R13) Advanced Supplementary Examinations July 2018

RF INTEGRATED CIRCUITS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Write the conditions for resonance in parallel RLC network.
(b) What is reflection coefficient in RF system?
(c) What is the relation between bandwidth and rise time for 1st order systems?
(d) What is figure of merit for a MOS devices?
(e) Define noise figure.
(f) What is mixer? Why the uses of mixer?
(g) What is meant by negative resistance oscillators?
(h) What is the difference between filter and loop filter?
(i) Define phase noise.
(j) What is CDMA?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Explain in detail 'Pi' and 'T'-matching of a network.
(b) Explain in detail the basic architecture of a RF system.

OR

3 (a) Compare parallel RLC and series RLC networks.
(b) Explain about passive IC components interconnects in detail.

UNIT – II

4 (a) Draw and explain about shunt-series amplifier and write its applications.
(b) Draw and explain about CS-amplifier for a single tuned amplifier.

OR

5 Explain and derive bandwidth estimation using open circuit time constant and short circuit time constant.

UNIT – III

6 (a) Discuss about thermal noise, flicker noise and noise figure.
(b) Explain in detail LNA design.

OR

7 Explain about mixer design and sub sampling mixers.

UNIT – IV

8 (a) Explain about class A, AB RF power amplifier with neat diagrams.
(b) Explain about charge pumps and loop filters.

OR

9 Write short notes on:
(a) Voltage controlled oscillators.
(b) Negative resistance oscillators.

UNIT – V

10 (a) Explain about GSM radio architectures in detail with suitable diagram.
(b) Discuss about integer-N synthesis and fractional frequency synthesis.

OR

11 Write short notes on:
(a) UMTS radio architectures.
(b) CDMA radio architectures.

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PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Brief about behavior of wire at radio frequencies.
(b) Write a note on Q factor of parallel RLC circuit.
(c) Differentiate between distributed and lumped systems.
(d) Define rise time and delay time.
(e) Write noise figure equation.
(f) List different types of multiplier - based mixers.
(g) Draw the block diagram of General power amplifier model.
(h) which amplifier is introduced to overcome the crossover distribution that occurs in class B.
(i) List different types of resonator technologies.
(j) Draw the block diagram of generic transceiver.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain in detail about the architecture of Radio Frequency system.

OR

3 Define the T-match circuit and find out the net Q factor of the circuit.

UNIT – II

4 Derive an expression for characteristic impedance and propagation constant of lossy transmission line.

OR

5 Discuss the method of open circuit time constant for estimating the bandwidth of the system.

UNIT – III

6 Discuss the behavior of LNA topologies with its design constraints.

OR

7 Discuss in detail about sub sampling mixers.

UNIT – IV

8 Explain the operation of class A power amplifier and find its maximum drain efficiency.

OR

9 Explain in detail about linearized PLL models.

UNIT – V

10 Draw the block diagram of GSM radio architecture and explain brief.

OR

11 Explain the following:

(a) PLL.
(b) Charge pumps.

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Code: 13A04804 **R13**

B.Tech IV Year II Semester (R13) Regular Examinations April 2017

RF INTEGRATED CIRCUITS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What are the conditions for resonance in parallel RLC network?
(b) What is skin effect?
(c) Define reflection coefficient.
(d) State the relation between bandwidth and rise time for first order system.
(e) Write a note on excess noise.
(f) What is the advantage of sub sampling mixer?
(g) List the applications of PLL.
(h) Why is the isolator placed at the output of the amplifier?
(i) Write a note on ring oscillator.
(j) Define frequency synthesizer.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain in detail about the architecture of Radio Frequency system.

OR

3 Explain transmission medium and reflections in radio frequency system.

UNIT – II

4 Prove that a long channel MOSFET transconductance depends only on the square root of bias current.

OR

5 Discuss the method of short circuit time constant for estimating the bandwidth of the system

UNIT – III

6 Discuss in detail about FLICKER noise in MOSFETs.

OR

7 Briefly explain the mixer design considerations.

UNIT – IV

8 Explain in detail about class F amplifiers.

OR

9 Explain about different negative resistance oscillators with neat sketch.

UNIT – V

10 Explain the method of frequency synthesis using fractional – N synthesizers.

OR

11 Draw the block diagram of UMTS radio architecture and explain in detail.

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Code: 13A04804 **R13**

B.Tech IV Year II Semester (R13) Regular & Supplementary Examinations April 2018

RF INTEGRATED CIRCUITS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) State the maximum power transfer theorem and its conditions.
(b) What are the conditions for resonance in series RLC networks?
(c) Define gain and bandwidth.
(d) What is reflection coefficient?
(e) What is thermal noise?
(f) Define phase locked loop.
(g) What is power match and noise match.
(h) Define phase detector.
(i) What is meant by integer-N synthesis?
(j) Define frequency synthesis.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Design and convert series to parallel RL & RC network transformations.
(b) Explain about passive IC components interconnects in RF system.

OR

3 (a) Compare Pi match and T-match of a network system.
(b) Discuss about the basic architecture of a RF system.

UNIT – II

4 Prove that a long channel MOS device transconductance depends only on the square root of bias current.

OR

5 (a) Draw and explain about the tuned amplifier.
(b) Explain about the high frequency amplifier design.

UNIT – III

6 (a) Explain about intrinsic MOS noise parameters.
(b) Explain about power match versus noise match.

OR

7 Design any two examples of multiplier based mixers.

UNIT – IV

8 (a) Discuss about class D, E, F amplifier in detail.
(b) Explain about phase locked loops and phase detectors.

OR

9 Write short notes on:
(a) Negative resistance oscillators.
(b) Linearlized PLL models.

UNIT – V

10 (a) Explain about frequency synthesis in detail.
(b) Discuss about phase noise and fractional frequency in frequency synthesis.

OR

11 Write short notes on:
(a) GSM radio architecture.
(b) CDMA radio architecture.

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Code: 15A04804

R15

B.Tech IV Year II Semester (R15) Regular Examinations April 2019

RF INTEGRATED CIRCUITS

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Draw a series RLC tank circuit.

(b) Differentiate between series and parallel RLC networks.

(c) What is the range of reflection coefficient?

(d) A cascade of 8 identical amplifiers is connected in open circuit, each of which is single-pole with a 2 ms time constant. Find its bandwidth.

(e) For a 1 kΩ resistor at room temperature and a 10 kHz bandwidth, find the RMS noise voltage.

(f) Write a note on subsampling mixers.

(g) The average power delivered to the load is given as 10 W, P_{in} = 2 W and P_{supp} = 4 W, find the power-added efficiency of the power amplifier.

(h) Give the average current and average slope equation of PFD/CP circuit for an input phase difference of $\Delta\phi\ rad = [\Delta\phi/2\pi] \times T_{in}$.

(i) With the phase noise –40dBc integrated over the range of 1 kHz to 100 kHz. Give the expression to convert it in to jitter.

(j) Mention some advantages of UMTS radio architectures.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Derive the expression for Q factor in an RLC network with a neat diagram and necessary equations.

OR

3 What is the role of resistors, capacitors and inductors in an RF system? Explain in detail.

UNIT – II

4 A slotted line measurement yields the following parameter values:
(i) Voltage minima at 9.2 cm and 12.4 cm measured away from the load with the line terminated in a short.
(ii) VSWR = 5.1 with the line terminated in the unknown load; a voltage minimum is located 11.6 cm measured away from load. What is the normalized line impedance?

OR

5 Consider an AC-coupled system to estimate the low frequency -3dB point. Calculate that how large the coupling capacitors have to be to achieve a specified low-frequency breakpoint.

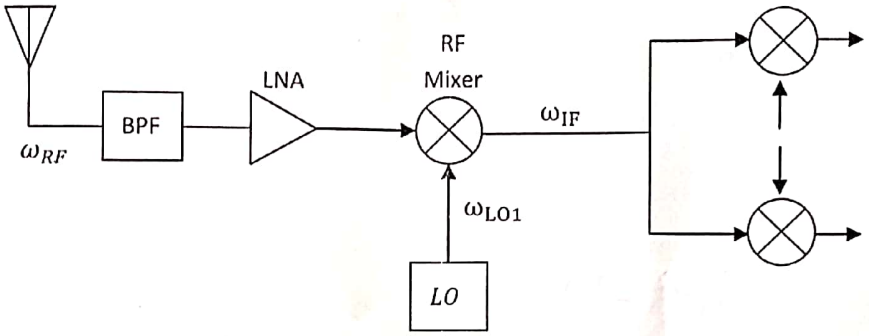
Contd. in page 2

UNIT – III

6 What are the parameters associated with intrinsic MOS noise? Explain in detail about each one of them with necessary equations.

OR

7 Discuss the noise behavior of the following receiver in two cases shown in figure given below:
(i) ω_{LO1} is far from ω_{RF}.
(ii) ω_{LO1} lies inside the band.



UNIT – IV

8 Construct a tank consisting of lossy inductor and lossy capacitor. Determine the overall Q in terms of the quality factor of each.

OR

9 Plot the input / output characteristic of the XOR phase detector for two cases:
(i) The circuit has a single-ended output that swings between 0 to V_{DD}.
(ii) The circuit has a differential output that swings between $-V_0$ and $+V_0$.

UNIT – V

10 Derive the expression for randomization and noise shaping in a fractional-N frequency synthesizers.

OR

11 Give a brief note on the following radio architectures:
(a) Code Division Multiple Access.
(b) Universal Mobile Telecommunication System.

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