UNIT-III

GATE LEVEL DESIGN

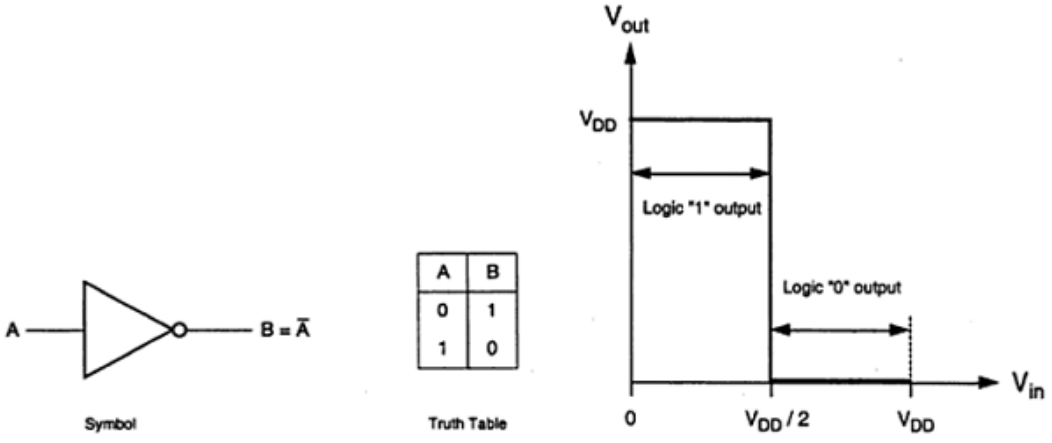
LOGIC GATES AND OTHER COMPLEX GATES:

- Invert(nmos, cmos, Bicmos)
- NAND Gate(nmos, cmos, Bicmos)
- NOR Gate(nmos, cmos, Bicmos)

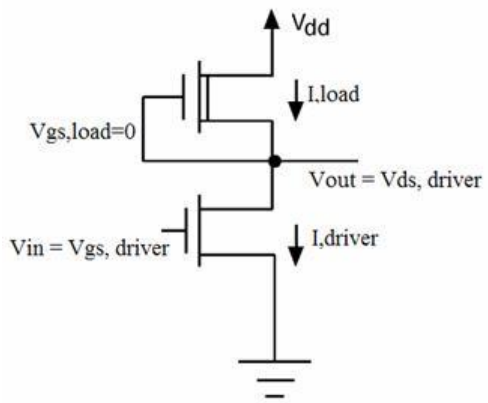
The module (integrated circuit) is implemented in terms of logic gates and interconnections between these gates. Designer should know the gate-level diagram of the design. In general, gate-level modeling is used for implementing lowest level modules in a design like, full-adder, multiplexers, etc.

nmos Inverter : The logic symbol and truth table of ideal inverter is shown in figure given below. Here A is the input and B is the inverted output represented by their node voltages. Using positive logic, the Boolean value of logic 1 is represented by V_{dd} and logic 0 is represented by 0. V_{th} is the inverter threshold voltage, which is V_{dd} /2, where V_{dd} is the output voltage.

The output is switched from 0 to V_{dd} when input is less than V_{th}. So, for $0<V_{in}<V_{th}$ output is equal to logic 0 input and $V_{th}<V_{in}< V_{dd}$ is equal to logic 1 input for inverter.



The characteristics shown in the figure are ideal. The nmos inverter is as shown



Let us consider the nmos inverter with 8:1 pull up transistors and 1:1 pull down transistors. Using this data, the power dissipated by the inverter is obtained as

$$R_{pu} = Z_{pu} * R_s = 8*10\text{Kohms} = 80\ k\Omega$$

$$R_{pd} = Z_{pd} * R_s = 1*10\text{Kohms} = 10\ k\Omega$$

Assuming $V_{dd} = 5V$

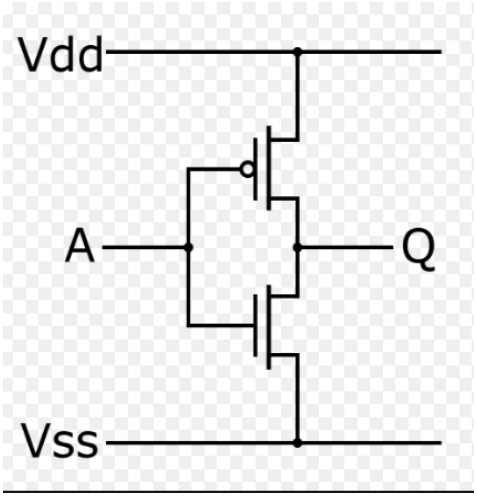
(Power dissipated) $P_d = V^2/(R_{pu} + R_{pd})$

$=25/(90\ K\ \Omega)$

$=o.28\ nW$

Further, as the pull down transistors shape-factor is '1', the input capacitance is 1 C_g.

cmos Inverter : The CMOS inverter circuit is shown in the figure. Here, nMOS and pMOS transistors work as driver transistors; when one transistor is ON, other is OFF.



This configuration is called **complementary MOS (CMOS)**. The input is connected to the gate terminal of both the transistors such that both can be driven directly with input voltages. Substrate of the nMOS is connected to the ground and substrate of the pMOS is connected to the power supply, V_{DD}.

So $V_{SB} = 0$ for both the transistors.

$$VGS,n=VinVGS,n=Vin$$

$$VDS,n=VoutVDS,n=Vout$$

And,

$$VGS,p=Vin−VDDVGS,p=Vin−VDD$$

$$VDS,p=Vout−VDDVDS,p=Vout−VDD$$

When the input of nMOS is smaller than the threshold voltage ($V_{in} < V_{TO,n}$), the nMOS is cut − off and pMOS is in linear region. So, the drain current of both the transistors is zero.

ID,n=ID,p=0ID,n=ID,p=0

Therefore, the output voltage V_{OH} is equal to the supply voltage.

Vout=VOH=VDDVout=VOH=VDD

When the input voltage is greater than the $V_{DD} + V_{TO,p}$, the pMOS transistor is in the cutoff region and the nMOS is in the linear region, so the drain current of both the transistors is zero.

ID,n=ID,p=0ID,n=ID,p=0

Therefore, the output voltage V_{OL} is equal to zero.

Vout=VOL=0Vout=VOL=0

The nMOS operates in the saturation region if $V_{in} > V_{TO}$ and if following conditions are satisfied.

VDS,n≥VGS,n−VTO,nVDS,n⩾VGS,n−VTO,n

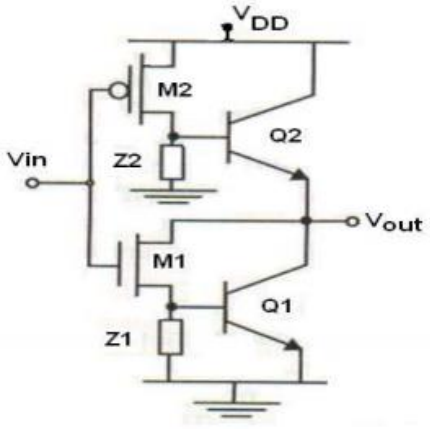
Vout≥Vin−VTO,nVout⩾Vin−VTO,n

The pMOS operates in the saturation region if $V_{in} < V_{DD} + V_{TO,p}$ and if following conditions are satisfied.

VDS,p≤VGS,p−VTO,pVDS,p⩽VGS,p−VTO,p

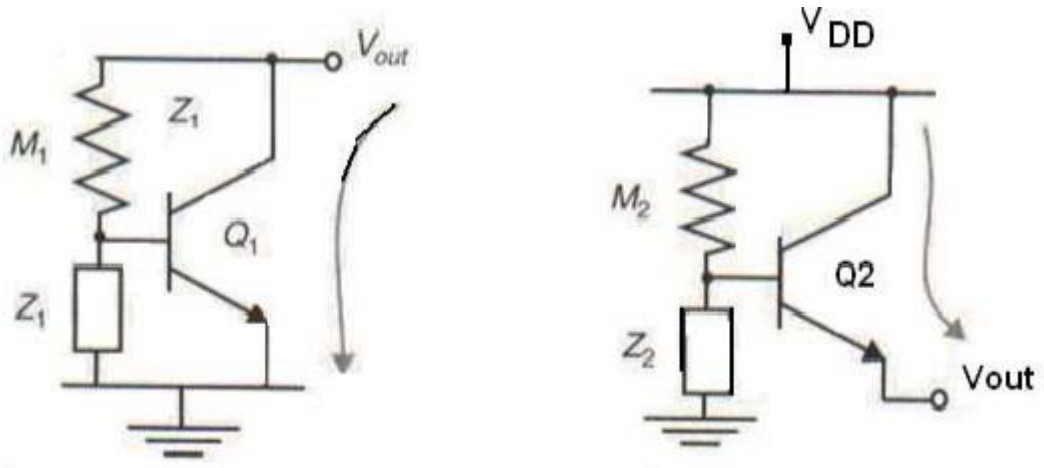
Vout≤Vin−VTO,p

bicmos Inverter : A BiCMOS inverter, consists of a PMOS and NMOS transistor (M2 and M1), two NPN bipolar junction transistors,(Q2 and Q1), and two impedances which act as loads(Z2 and Z1) as shown in the circuit below.



When input, Vin, is high (VDD), the NMOS transistor (M1), turns on, causing Q1 to conduct,while M2 and Q2 are off, as shown in figure (b) . Hence , a low (GND) voltage is translated to the output Vout. On the other hand, when the input is low, the M2 and Q2 turns on, while M1and Q1 turns off, resulting to a high output level at the output as shown in Fig.(b). In steady-state operation, Q1 and Q2 never turns on or off simultaneously, resulting to a lower power consumption. This leads to a push-pull bipolar output stage.

Transistors M1and M2, on the other hand, works as a phase-splitter, which results to a higher input impedance.



The impedances Z2 and Z1 are used to bias the base-emitter junction of the bipolar transistor and to ensure that base charge is removed when the transistors turn off. For example when the input voltage makes a high-to-low transition, M1 turns off first. To turn off Q1, the base charge must be removed, which can be achieved by Z1.With this effect, transition time reduces. However, there exists a short time when both Q1 and Q2 are on, making a direct path from the supply (VDD) to the ground. This results to a current spike that is large and has a detrimental effect on both the noise and power consumption, which makes the turning off of the bipolar transistor fast .

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nmos NAND Gate :

$v_{out} <= v_t = 0.2v_{dd}$

$V_{out} = (v_{dd}*n*z_{pd})/(nz_{pd}+z_{pu}) = 0.2v_{dd}$

$= (nz_{pd})/(nz_{pd}+z_{pu}) = 0.2$

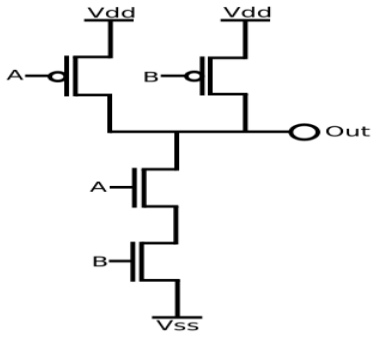
Consider $z_{pd} = 1$

$(2)/(2+z_{pu}) = 0.2$

$0.2z_{pu} = 2-0.4$

$Z_{pu}= 8$

$(z_{pu})/(2*z_{pd}) = 8/2 = 4$



nmos NAND geometry reveals two significant factors:

--nmos NAND gate area requirements are greater than those of a corresponding nmos inverter, pull down transistors must be added in series to provide no.of inputs, as inputs are added there must be corresponding length adjustment of pull up transistor, channel to maintain required overall ratio.

--nmos NAND gate delays are also increased in direct proportion to the members of required added. If pull down transistor are kept at minimum size (2λx2λ) each will present 10's CG at its inputs. But if their n such inputs then the length and resistance by a factor n to keep correct ratio. Thus the delay associated with nmos NAND are

$T_{NAND} = \eta\, T_{inv}$

Where , n- No. Of inputs

T_{inv} - Inverted delay

Other approach, keeping Z_{pu} constant and widening pull down channels.

Nmos NAND gate is used only where absolutely necessary and when the number of inputs are restricted.

cmos NAND Gate : The two input NAND function is expressed by Y=A.B

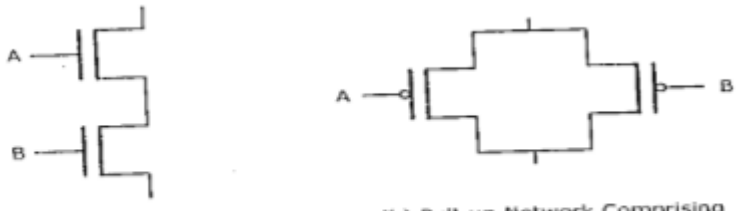
Step 1 Take complement of Y

Y= A.B = A.B

Step 2 Design the PDN

In this case, there is only one AND term, so there will be two nMOSFETs in series as shown in figure.

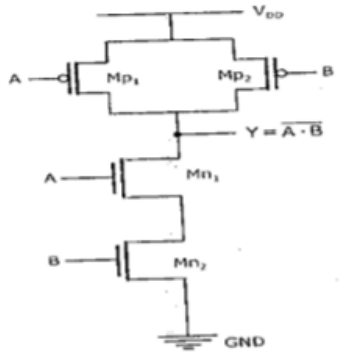
Step 3 Design the PUN. In PUN there will be two pMOSFETs in parallel , as shown in figure



(a) Pull-down Network Comprising nMOSFETs

(b) Pull-up Network Comprising pMOSFETs

Finally join the PUN and PDN as shown in figure which realizes two – input NAND gate. Note that we have realized y, rather tat Y because the inversion is automatically provided by the nature of the CMOS circuit operation,



Working operation

1) Whenever at least one of the inputs is LOW, the corresponding pMOS transistor will conduct while the corresponding nMOS transistor will turn OFF. Subsequently, the output voltage will be HIGH.

2) Conversely, if both inputs are simultaneously HIGH, then both pMOS transistors will turn OFF, and the output voltage will be pulled LOW by the two conducting nMOS transistors.

The cmos NAND gate has no such restrictions but, bearing in mind the remarks are asymmetry, it is necessary to allow for extended fall times on capacitive loads owing to the no.of n-transistors in series forming the pull down. Some adjustments of transistor geometry is necessary for this reason and to keep the transfer characteristics symmetrical above $v_{dd}/2$.

bicmos NAND Gate : The bicmos gate is shown in practical version and is thus more complex than the simple intuitive version. However, it has considerable load driving capabilities and is most useful where a large fan out is required or where there is some other form of high capacitance load on the output. A typical mask layout for this gate, using orbit^{TM} 2µm design rules, is given in monochrome form.

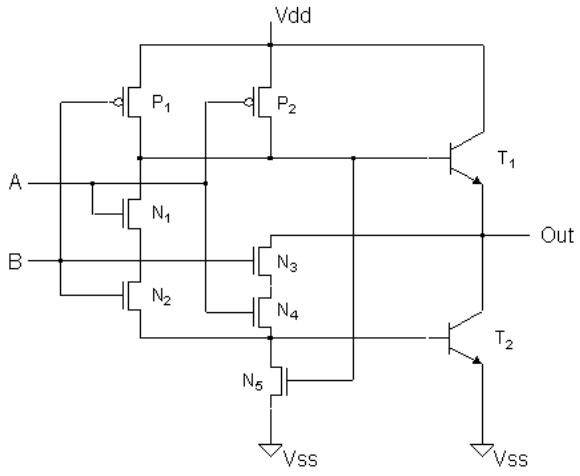


Figure 8.1: The BICMOS nand gate circuit.

nmos NOR Gate :

NOR gate can be used to accommodate any reasonable number of inputs (preferred over nand gate).

Both legs of two input nmos nor gate provided.

The ratio must be such that one conducting pull down leg will give inverted line transfer characteristics.

Ares occupied by nmos NOR gate is reasonable since the pull up transistor dimensions are unaffected by the number of inputs accommodate.

NOR gate is as fast as the inverter and is the preferred inverted based nmos logic.

cmos NOR Gate : The two input NOR function is expressed by

$$Y=A+B$$

Step 1: Take complement of Y

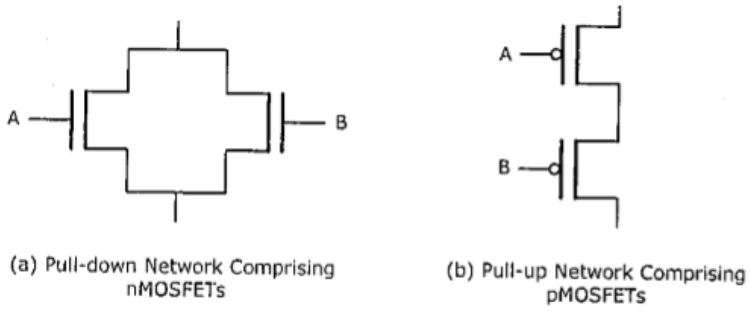
$$Y= A+B = A+B$$

Step 2: Design the PDN

In this case, there is only one OR term, so there will be two nMOSFETs connected in parallel, as shown in figure.

Step 3: Design the PUN

In PUN there will be two pMOSFETs in series , as shown in figure



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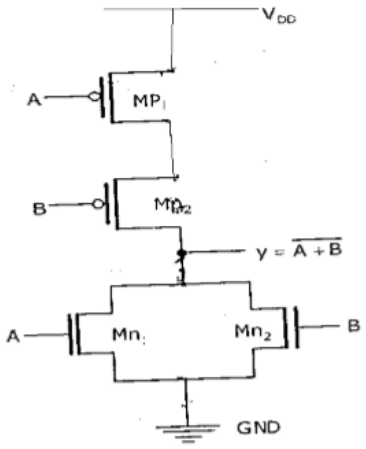


Two pull up transistors are required to implement the logic '1' condition and two pull down transistors are required to implement logic '0'.

Pmos are connected in series, nmos are connected in parallel.

Predominant resistance of the p-devices is aggravated in its effect by the number connected in series.

Raise and fall time asymmetry on capacity load is increased and there will be a shift in the transfer characteristics which will reduce noise immunity.

For these reasons CMOS NOR gate with more than 2 inputs may require adjustment if p,n transistors geometry.

SWITCH LOGIC:

1) Switch logic is mainly based on pass transistor or transmission gate.

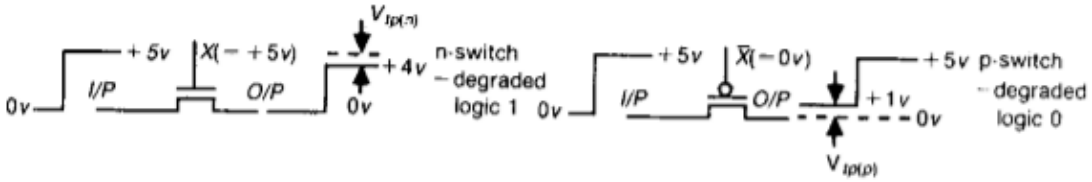
2) It is fast for small arrays and takes no static current from the supply, VDD. Hence power dissipation of such arrays is small since current only flows on switching.

3) Switch (pass transistor) logic is analogous to logic arrays based on relay contacts, where in path through each switch is isolated from the logic levels activating the switch.

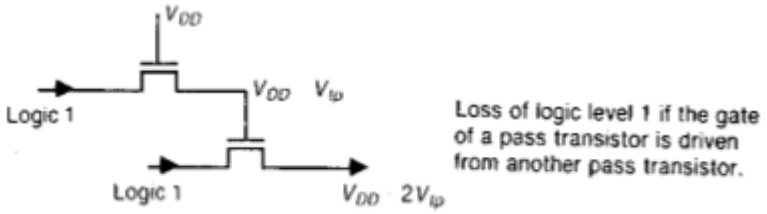
PASS TRANSISTOR:

1) This logic uses transistors as switches to carry logic signals from node to node instead of connecting output nodes directly to VDD or ground(GND)

2) If a single transistor is a switch between two nodes, then voltage degradation.equal to Vt(threshold voltage) for high or low level depends up on nMOS or pMOS logic.



3) When using nMOS switch logic no pass transistor gate input may be driven through one or more pass transistors as shown in figure.



4) Since the signal out of pass transistor T1 does not reach a full logic 1 by threshold voltage effects signal is degraded by below a true logic 1, this degraded voltage would not permit the output of T2 to reach an acceptable logic 1 level.

Advantages

They have topological simplicity.

1) Requires minimum geometry.

2) Do not dissipate standby power, since they do not have a path from supply to ground.

Disadvantages

1) Degradation in the voltage levels due to undesirable threshold voltage effects.
2) Never drive a pass transistor with the output of another pass transistor.

TRANSMISSION GATE :

1) It is an electronic element, good non-mechanical relay built with CMOS technology.

2) It is made by parallel combination of an nMOS and pMOS transistors with the input at gate of one transistor being complementary to the input at the gate of the other as shown in figure.

3) Thus current can flow through this element in either direction.

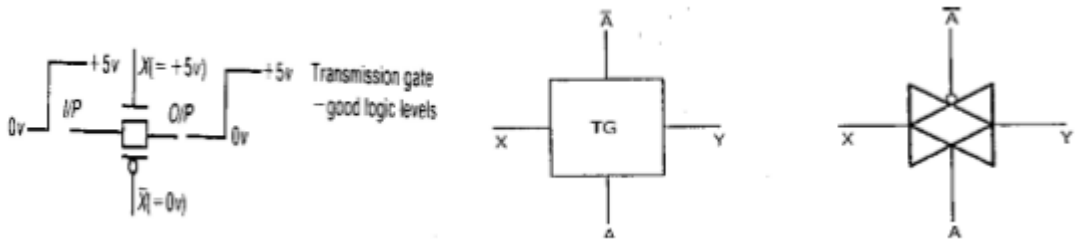
4) Depending on whether or not there is a voltage on the gate, the connection between the input and output is either low resistance or high-resistance, respectively Ron = 100Ω and Roff > 5 MΩ.

Operation

• When the gate input to the nMOS transistor is ‘0’ and the complementary ‘1’ is gate input to the pMOS , thus both are turned off.

• When gate input to the nMOS is ‘1’ and its complementary ‘0’ is the gate input to the pMOS , both are turned on and passes any signal ‘1’ and ‘0’ equally without any degradation.

• The use of transmission gates eliminates the undesirable threshold voltage effects which give rise to loss of logic levels in pass-transistors as shown in figure.



Advantages

1) Transmission gates eliminates the signal degradation in the output logic levels.

2) Transmission gate consists of two transistors in parallel and except near the positive and negative rails.

Disadvantages

1) Transmission gate requires more area than nMOS pass circuitry.

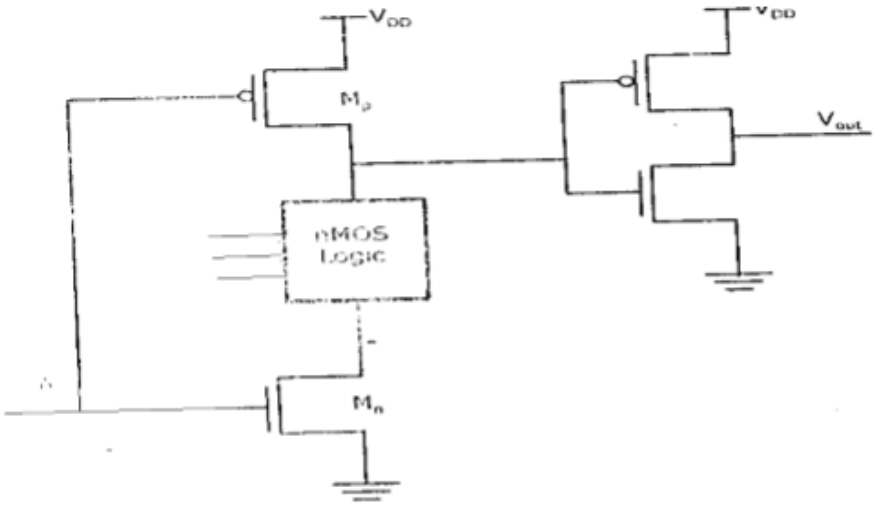
2) Transmission gate requires complemented control signals.

CMOS DOMINO LOGIC

Standard CMOS logic gates need a PMOS and an NMOS transistor for each logic input. The pMOS transistors require a greater area tan the nMOS transistors carrying the same current. So, a large chip area is necessary to perform complex logic operations. The package density in CMOS is improved if a dynamic logic circuit, called the domino CMOS logic circuit, is used.

Domino CMOS logic is slightly modified version of the dynamic CMOS logic circuit. In this case, a static inverter is connected at the output of each dynamic CMOS logic block. The addition of the inverter solves the problem of cascading of dynamic CMOS logic circuits.

The circuit diagram of domino CMOS logic structures as shown in figure as follows



A domino CMOS AND-OR gate that realizes the function y = AB + CD is depicted in fugure . The left hand part of the circuit containing Mn,Mp, T1,T2,,T3,and T4 forms and AND-ORINVERTER (AOI) gate. It derives the static CMOS inverter formed by N2 and P2 in the right

hand part of the circuit. The domino gate is activated by the single phase clock ø applied to the NMOS (Mn) and the PMOS (Mp) transistors. The load on the AOI part of the circuits is the parasitic load capacitance.

Working

• When ø = 0, is ON and Mn is OFF, so that no current flows in the AND-OR paths of the AOI. The capacitor CL is charged to VDD through Mp since the latter is ON. The input to the inverter is high, and drives the output voltage V0 to logic-0.

• When ø = 1, Mp is turned OFF and Mn is turned ON. If either (or both) A and B or C and D is at logic-1, CL discharges through either T2,T1 and Mn or T3,T4 and Mp. So , the inverter input is driven to logic-0 and hence the output voltage V0 to logic-1. The Boolean expression for the output voltage is Y = AB + CD.

Note : Logic input can change only when ø = 0. No changes of the inputs are permitted when ø = 1 since a discharge path may occur.

Advantages

1) Smaller areas compared to conventional CMOS logic.

2) Parasitic capacitances are smaller so that higher operating speeds are possible.

3) Operation is free of glitches since each gate can make one transition.

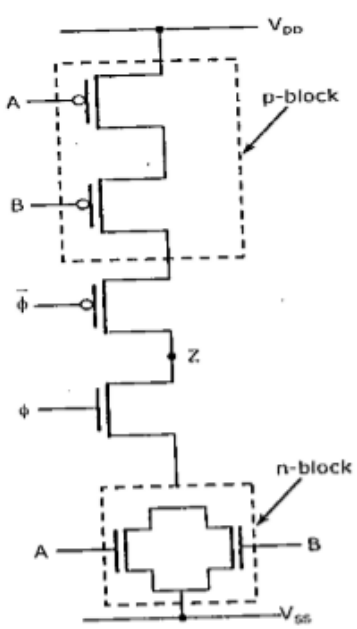
Disadvantages

1) Non inverting structures are possible because of the presence of inverting buffer.

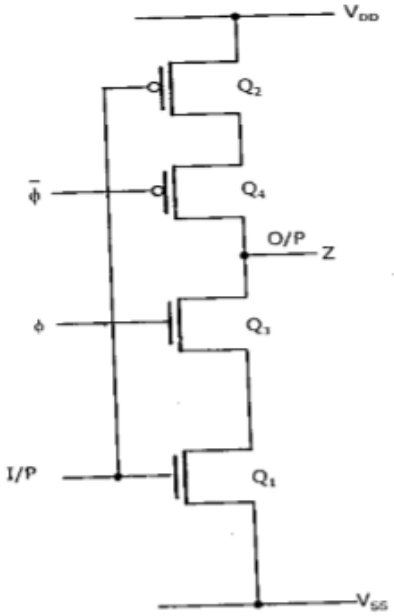
2) Charge distribution may be a problem.

CLOCKED CMOS LOGIC :

The clocked CMOS logic is also referred as C2MOS logic. Figure shows the general arrangement of a clocked CMOS (C2MOS) logic. A pull-up p-block and a complementary n-block pull-down structure represent p and n-transistors respectively and are used as implement clocked CMOS logic shown in figure. However, the logic in this case is connected to the output only during the ON period of the clock. Figure shows a clocked inverter circuit which is also belongs to clocked CMOS logic family. The slower rise times and fall times can be expected due to owing of extra transistors in series with the output.



(a) Implemented CMOS Logic



(b) Clocked Inverter Circuit

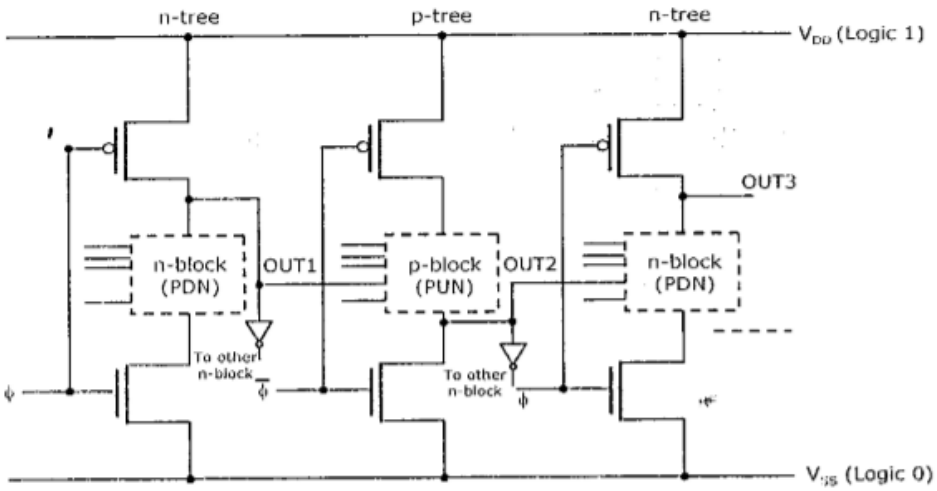
Working

• When ø = 1 the circuit acts an inverter , because transistors Q3 and Q4 are ‘ON’ . It is said to be in the “evaluation mode”. Therefore the output Z changes its previous value.

• When ø = 0 the circuit is in hold mode, because transistors Q3 and Q4 becomes ‘OFF’ . It is said to be in the “precharge mode”. Therefore the output Z remains its previous value

n-p CMOS LOGIC :

Figure shows the another variation of basic dynamic logic arrangement of CMOS logic called as n-p CMOS logic. In this, logic the actual logic blocks are alternatively ‘n’ and ‘p’ in a cascaded structure. The clock ø and ø- are used alternatively to fed the precharge and evaluate transistors. However, the functions of top and bottom transistors are also alternate between precharge and evaluate transistors.



Working

• During the pre charge phase ø = 0 , the output of the n-tree gate, OUT 1 OUT3 , are charged to VDD, while the output of the p-tree gate OUT2 is pre discharged to 0V. Since the n-tree gate connects pMOS pull-up devices, the PUN of the p-tree is turned off at that time.

• During the evaluation phase ø = 1, the outputs (OUT1,OUT3) of the n-tree gate can only make a 1-Æ0 transition, conditionally turning on some transistors in the p-tree. This ensures that no accidental discharge of OUT 2 can occur.

• Similarly n-tree blocks can follow p-tree gates without any problems, because the inputs to the n-gate are pre charged to 0.

Disadvantages

Here, the p-tree blocks are slower than the n-tree modules, due to the lower current drive of the pMOS transistors in the logic network.