Code: 13A04306

R13

B.Tech II Year I Semester (R13) Regular Examinations December 2014

DIGITAL LOGIC DESIGN

(Common to IT and CSE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) If $1010_2 + 10_2 = X_{10}$, then X is -----

(b) Write the first 9 decimal digits in base 3.

(c) What is meant by don't care condition?

(d) Why AND and OR are not universal gates? Give the reason.

(e) Write the truth table of half subtractor.

(f) Implement AND gate using only two input NOR gates.

(g) Write the truth table of clocked T-Flip flop.

(h) Where the ripple counter is used?

(i) What is the function of EAROM?

(j) Mention few applications of PAL.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT - I

2 (a) Obtain the truth table for the function F = xy + xy' + y'z

(b) Prove that the sum of all minterms of a Boolean function for three variables is 1.

OR

3 (a) Show that the dual of the exclusive-OR is equal to its complement

(b) Convert the decimal number 1973 to base 3, base 5 and base 7.

UNIT - II

4 Simplify the following Boolean expressions using K-map and implement them using NAND gates:
F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ.

OR

5 Simplify the following expression using tabulation method:
F(A, B, C, D, E) = ∑ (4, 6, 7, 9, 11, 12, 13, 14, 15, 20, 22, 25, 27, 28, 30) + d(1, 5, 29, 31).

UNIT - III

6 (a) How full adder is different from full subtractor? Explain.

(b) Draw and explain various implementations of full adder.

OR

7 (a) What is the function of magnitude comparator? Explain with an example.

(b) Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit.

UNIT - IV

8 (a) Draw the block diagram of sequential circuit. Explain.

(b) What is state assignment? Explain with a suitable example.

OR

9 (a) Draw the basic flip flop circuit with NOR gates. Explain its operation.

(b) Explain about 3-bit binary counter with a suitable logic diagram.

UNIT - V

10 (a) Compare PAL and PLA with respect to various performance features.

(b) Explain about TTL family.

OR

11 (a) Explain about memory decoding error detection and correction.

(b) What is the importance of ECL family? Explain.

*****

Code: 13A04306 **R13**

B.Tech II Year I Semester (R13) Regular & Supplementary Examinations December 2015

DIGITAL LOGIC DESIGN

(Common to IT and CSE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Determine the value of base 'X' if $(225)_x = (341)_8$.
(b) Find the complement of the function, F = x (y'z' + yz) by taking their duals and complementing each literal.
(c) Define don't care condition with an example.
(d) Implement EX-OR gate using only NAND gates.
(e) Define priority encoder.
(f) Give the design procedure for the design of a combinational circuit.
(g) What is race around condition? How can we eliminate the race around condition?
(h) Define shift registers.
(i) What are the differences between PLA and PAL?
(j) Define fan out of a logic gate.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT - I

2 (a) Convert the following $(3456)_8$ to base 3 and base 7.
(b) Using 2's complement, perform $(42)_{10}$-$(68)_{10}$

OR

3 (a) Simplify the following three variable expression using Boolean algebra: Y = ∑m(1, 3, 5, 7).
(b) Convert the given expression in standard POS form: Y = A.(A + B + C)

UNIT - II

4 (a) Minimize the following function using Karnaugh map method.
f(w,x,y,z)= ∑m(0,7,8,9,10,12) + ∑d (2,5,13)
(b) Implement the following function in NAND-NAND two level forms and draw the circuits.
Y = AC+ABC+A'BC+AB+D

OR

5 Minimize the following function using tabular method.
f(A,B,C,D) = ∑m(0,1,9,15,24,29,30) + ∑d (8,11,31)

UNIT - III

6 (a) Design and draw a full adder circuit.
(b) Implement the following Boolean function using 4 x 1 MUX.
F(a,b,c) = ∑m (1,3,5,6)

OR

7 Design 2 bit magnitude comparator and draw its logic circuit diagram.

UNIT - IV

8 (a) Draw and explain the operation of RS flip-flop.
(b) Design and draw the 3 bit up-down synchronous counter.

OR

9 What are the different types of shift registers? Explain any one type of shift register.

UNIT - V

10 Implement the following functions using PLA.

A (x,y,z)= ∑m (1,2,4,6)
B (x,y,z) = ∑m (0,1,6,7)
C (x,y,z) = ∑m (2,6)

OR

11 (a) Differentiate between RAM and ROM.
(b) Draw and explain the operation of 2 input TTL NAND gate with totem pole output.

*****

Code: 13A04306 **R13**

B.Tech II Year I Semester (R13) Supplementary Examinations June 2017

DIGITAL LOGIC DESIGN

(Common to CSE & IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Reduce AB + (AC)' + AB'C (AB + C).

(b) Simplify the following expression Y = (A + B)(A + C')(B' + C').

(c) Define K-map? Name its advantages and disadvantages.

(d) Write about universal logic gates and realize XOR gate using Universal gates.

(e) Construct full adder using half adders.

(f) Compare a decoder with a Demultiplexer.

(g) What is race around condition?

(h) Write about bidirectional shift register.

(i) List basic types of programmable logic devices.

(j) Explain about parallel in serial out shift register.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Convert 1A53 Hexadecimal to its decimal equivalent.

(b) Convert $(734)_8$ to its hexadecimal equivalent.

(c) Convert 0.640625 decimal number to its octal equivalent.

(d) Convert 0.1289062 decimal number to its hex equivalent.

OR

3 Prove the following identities:

(i) A' B' C' + A' B C' + A B' C' + A B C' = C'.

(ii) A B + A B C + A' B + A B' C = B + A C.

UNIT – II

4 A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations

a) A is False b) A, B, C are True

(i) Write the Truth table for F. Use the convention True = 1 and False = 0.

(ii) Write the simplified expression for F in SOP form.

(iii) Write the simplified expression for F in POS form.

(iv) Draw logic circuit using minimum number of 2-input NAND gates.

OR

5 Simplify the following expression into sum of products using Karnaugh map:

F(A, B, C, D) = ∑(1, 3, 4, 5, 6, 7, 9, 12, 13)

UNIT – III

6 Draw and explain the working of a carry-look ahead adder.

OR

7 (a) Design a 4-bit adder-subtractor circuit and explain the operation in detail.

(b) Explain the functionality of a decoder.

Contd. in page 2

UNIT – IV

8 Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.

OR

9 Define a register. Construct a shift register from S-R flip-flops. Explain its working.

UNIT – V

10 (a) Compare PLA with PROM.

(b) What is ROM? List the different types of ROMs.

OR

11 Write about the following:

(a) CMOS logic.

(b) Digital logic circuits.

*****

Code: 15A04306 **R15**

B.Tech II Year I Semester (R15) Supplementary Examinations June 2017

DIGITAL LOGIC DESIGN

(Common to CSE and IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) If $143_5 = X_6$, then X is -----

(b) What is meant by binary logic?

(c) Implement Y = A + B C using minimum number of two input NAND gates.

(d) What is the importance of prime implicants?

(e) What is problem of lock out in counters? Explain.

(f) What is the working principle of magnitude comparator?

(g) What is meant by Flip-Flop?

(h) Where the ripple counter is used? Explain.

(i) What is the function of EAROM?

(j) Draw the circuit diagram of TTL.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Convert the following to Decimal and then to Octal. (i) 4204_{16}. (ii) 1010011_2.

OR

3 Find the complement of the following Boolean function and reduce into minimum number of literals.
Y= (BC'+A'D)(DB'+CD')

UNIT – II

4 Using 5-variable k-map, find minimal SOP expressions for the following logic function:
F = ∑(0, 2, 4, 5, 6, 7, 8, 10, 17, 18, 21, 29, 31)+d(11, 20, 22)

OR

5 Simplify the following expression using tabulation method:
F(A,B,C,D,E)= ∑(0,1,2,3,4,5,10,11,14,20,21,24,25,26,27,28,29,30)

UNIT – III

6 Design 32:1 Multiplexer using two 16:1 Multiplexers and one 2:1 Multiplexer.

OR

7 (a) Design a 4 bit binary-to-BCD code converter.

(b) Briefly explain the operation of a carry look ahead adder

UNIT – IV

8 (a) Design and draw the logic diagram for MOD-6 ripple counter.

(b) How is the race around condition eliminated in JK Flip Flop?

OR

9 Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram.

UNIT – V

10 (a) Explain about MOS and CMOS logic.

(b) Explain about basic circuit and NOR of ECL with its characteristics.

OR

11 (a) Write short notes on PLA.

(b) Implement the following Boolean function using PLA:
$F_1(A,B,C) = ∑m(3,5,6,7)$
$F_2(A,B,C) = ∑m(0,2,4,7)$

*****