

B.Tech II Year II Semester (R13) Regular Examinations May/June 2015

COMPUTER ORGANIZATION & ARCHITECTURE

(Common to IT & CSE)

Time: 3 hours

Max. Marks: 70

PART – A
(Compulsory question)

- 1 Answer the following: (10 X 02 = 20 Marks)
- (a) Differentiate between computer organization and architecture.
 - (b) List any five assembly language instructions.
 - (c) What are the phases in instruction cycle?
 - (d) Define interrupt. List the types of interrupts.
 - (e) Write about register transfer notations.
 - (f) Give a note on control address registers.
 - (g) Cache memory is organized on what basis. List the advantages of using Cache memory.
 - (h) How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
 - (i) Draw the hyper cube structure for $n = 1, 2, 3$.
 - (j) What is the purpose of pipeline?

PART – B
(Answer all five units, 5 X 10 = 50 Marks)**UNIT – I**

- 2 List and explain the functional units of a computer with a neat diagram.
(OR)
- 3 Explain the computer levels of programming languages.

UNIT – II

- 4 What is an addressing mode? A two word instruction is stored in memory at an address designated by symbol W . The address field of the instruction (Stored at $W + 1$) is designated by the symbol Y . The operand used during the execution of the instruction is stored at an address symbolized by Z . An index register contains the value X . State how Z is calculated from the other addresses if the addressing mode of the instruction is: (i) Direct. (ii) Indirect. (iii) Relative. (iv) Indexed.
(OR)
- 5 Draw the flowchart for Booth's algorithm for multiplication of signed 2's complement numbers and explain with an example.

UNIT – III

- 6 (a) Draw and explain how to construct a bus line using three state buffers.
(b) How to multiply & divide a number by 2 using shift operations, give an example.
(OR)
- 7 Draw and explain the microprogram sequencer for a control memory.

UNIT – IV

- 8 The access time of a cache memory is 100 ns and that of main memory is 1000 ns. It is estimated that 80% of the memory requests are for read and the remaining 20% are for write. The hit ratio for read accesses only is 0.9. A write-through procedure is used.
- (a) What is the average access time of the system considering only memory read cycles?
 - (b) What is the average access time of the system for both read and write requests?
- (OR)
- 9 With a neat diagram, describe DMA transfer in a computer system.

UNIT – V

- 10 A nonpipeline system takes 50 ns to process a task. The same task can be processed in a 6 segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved.
(OR)
- 11 What are the various physical forms available for establishing an interconnection network? Explain.