RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations(20-21)
Branch: ECE

SET1

Sub: VLSI Design (15A04604) **Date: 21-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Define Moore's law. State various IC technologies on the basis of transistor count.	2	1	C314.1	Remember
1.ii.	Differentiate between PMOS and NMOS transistors.	2	1	C314.1	Analyze
1.iii.	Write about latch up and mention the remedy process to reduce it.	2	2	C314.2	Remember
1.iv.	What are the limitations of scaling	2	2	C314.2	Remember
1.v.	Design a simple NMOS NOR gate.	2	1	C314.2	Apply
2.	Draw V-I characteristics of NMOS transistor. Explain its operation.Derive the drain to source current equation in saturation and resistive region.	10	1	C314.1	Understand
3.a	Explain in detail the operation of nMOS inverter and draw its transfer characteristics.	5	1	C314.1	Understand
b.	What is figure of merit. Mention the suitable expressions for figure of merit.	5	1	C314.1	Remember
4a	What is a stick diagram and explain various symbols used for components in stick diagram.	5	2	C314.2	Understand
b	Discuss about VLSI design flow	5	2	C314.2	Understand
5.	Draw a stick diagram for two input nMOS NAND and NOR gates	10	2	C314.2	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations(20-21)
Branch: ECE

SET1

Sub: VLSI Design (15A04604) **Date: 21-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Define Moore's law. State various IC technologies on the basis of transistor count.	2	1	C314.1	Remember
1.ii.	Differentiate between PMOS and NMOS transistors.	2	1	C314.1	Analyze
1.iii.	Write about latch up and mention the remedy process to reduce it.	2	2	C314.2	Remember
1.iv.	What are the limitations of scaling	2	2	C314.2	Remember
1.v.	Design a simple NMOS NOR gate.	2	1	C314.2	Apply
2.	Draw V-I characteristics of NMOS transistor. Explain its operation.Derive the drain to source current equation in saturation and resistive region.	10	1	C314.1	Understand
3.a	Explain in detail the operation of nMOS inverter and draw its transfer characteristics.	5	1	C314.1	Understand
b.	What is figure of merit. Mention the suitable expressions for figure of merit.	5	1	C314.1	Remember
4a	What is a stick diagram and explain various symbols used for components in stick diagram.	5	2	C314.2	Understand
b	Discuss about VLSI design flow	5	2	C314.2	Understand
5.	Draw a stick diagram for two input nMOS NAND and NOR gates	10	2	C314.2	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations(20-21)
Branch: ECE

SET 2

Sub: VLSI Design (15A04604) **Date: 21-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Describe the operating regions for a MOS transistor.	2	1	C314.1	Remember
1.ii.	What is pass transistor?	2	1	C314.1	Understand
1.iii.	What is channel length modulation?	2	1	C314.1	Remember
1.iv.	Explain sheet resistance of a MOS device.	2	2	C314.2	Remember
1.v.	Impliment NOT gate using nMOS logic.	2	2	C314.2	Remember
2.	Explain NMOS fabrication process flow with neat diagrams..	10	1	C314.1	Understand
3.	Draw V-I characteristics of NMOS transistor. Explain its operation. Derive the drain to source current equation in saturation and resistive region	10	1	C314.2	Understand
4.a.	Write about design rules for wires	5	2	C314.2	Understand
b.	Draw the stick diagram and layout diagram for NOT gate in CMOS design style.	5	2	C314.2	Understand
5.a	Explain in detail rise time and fall time estimation of CMOS inverter delay.	5	2	C314.2	Understand
b	What do you mean by inverter delay? Explain	5	2	C314.2	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations(20-21)
Branch: ECE

SET 2

Sub: VLSI Design (15A04604) **Date: 21-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Describe the operating regions for a MOS transistor.	2	1	C314.1	Remember
1.ii.	What is pass transistor?	2	1	C314.1	Understand
1.iii.	What is channel length modulation?	2	1	C314.1	Remember
1.iv.	Explain sheet resistance of a MOS device.	2	2	C314.2	Remember
1.v.	Impliment NOT gate using nMOS logic.	2	2	C314.2	Remember
2.	Explain NMOS fabrication process flow with neat diagrams..	10	1	C314.1	Understand
3.	Draw V-I characteristics of NMOS transistor. Explain its operation. Derive the drain to source current equation in saturation and resistive region	10	1	C314.2	Understand
4.a.	Write about design rules for wires	5	2	C314.2	Understand
b.	Draw the stick diagram and layout diagram for NOT gate in CMOS design style.	5		C314.2	Understand
5.a	Explain in detail rise time and fall time estimation of CMOS inverter delay.	5	2	C314.2	Understand
b	What do you mean by inverter delay? Explain	5	2	C314.2	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations((20-21)
Branch: ECE

SET 3

Sub: VLSI Design (15A04604) **Date: 21-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Derive an expression for transconductance.	2	1	C314.1	Remembre
1.ii.	. Describe the different operating regions for a MOS transistor.	2	1	C314.1	Understand
1.iii.	Define stick diagram and design process.	2	2	C314.2	Remembre
1.iv.	What are the limitations of scaling.	2	2	C314.2	Remember
1.v.	Draw the logical circuit of two input CMOS NAND gate.	2	2	C314.2	Remember
2.	Design a CMOS inverter circuit and explain about its various region s of operation in detail with the necessary diagrams	10	1	C314.1	Understand,
3.	Derive the I_{DS}current equation at saturation and non-saturation regions.	10	1	C314.1	Understand
4 a b	Explain lambda based design rules Discuss about scaling factors for device parameters	5 5	2 2	C314.2 C314.2	Remember, Understand
5.a. b.	What is a stick diagram and explain different symbols used for components in stick diagram. Discuss about VLSI design flow	5 5	2 2	C314.2 C314.2	Apply, Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations((20-21)
Branch: ECE

SET 3

Sub: VLSI Design (15A04604) **Date: 21-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Derive an expression for transconductance.	2	1	C314.1	Remembre
1.ii.	. Describe the different operating regions for a MOS transistor.	2	1	C314.1	Understand
1.iii.	Define stick diagram and design process.	2	2	C314.2	Remembre
1.iv.	What are the limitations of scaling.	2	2	C314.2	Remember
1.v.	Draw the logical circuit of two input CMOS NAND gate.	2	2	C314.2	Remember
2.	Design a CMOS inverter circuit and explain about its various region s of operation in detail with the necessary diagrams	10	1	C314.1	Understand,
3.	Derive the I_{DS}current equation at saturation and non-saturation regions.	10	1	C314.1	Understand
4 a b	Explain lambda based design rules Discuss about scaling factors for device parameters	5 5	2 2	C314.2 C314.2	Remember, Understand
5.a. b.	What is a stick diagram and explain different symbols used for components in stick diagram. Discuss about VLSI design flow	5 5	2 2	C314.2 C314.2	Apply, Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations((20-21)
Branch: ECE

SET 4

Sub: VLSI Design (15A04604) **Date: 21-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	What is figure of merit. Mention the suitable expressions for figure of merit.	2	1	C314.2	Remember
1.ii.	Differentiate between PMOS and NMOS transistors..	2	1	C314.1	Remember
1.iii.	Define Moore's law. State various IC technologies on the basis of transistor count.	2	2	C314.2	Remember
1.iv.	Explain sheet resistance of a MOS device.	2	2	C314.2	Remember
1.v.	Design a simple NMOS NAND gate	2	1	C314.1	Remember
2.a. b.	Discuss about alternative forms of pull ups Explain the operation of BiCMOS inverter.	5 5	1 1	C314.1 C314.1	Remember Understand
3.	Describe the fabrication process of NMOS with neat sketches.	10	1	C314.1	Understand
4.a. b.	Discuss about NMOS design style Explain in detail rise time and fall time estimation of CMOS inverter delay	5 5	2 2	C314.2 C314.2	Remember Understand
5a. b	. What do you mean by inverter delay? Explain Discuss in detail VLSI design flow.	5 5	2 2	C314.3 C314.3	Understand Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations((20-21)
Branch: ECE

SET 4

Sub: VLSI Design (15A04604) **Date: 21-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	What is figure of merit. Mention the suitable expressions for figure of merit.	2	1	C314.2	Remember
1.ii.	Differentiate between PMOS and NMOS transistors..	2	1	C314.1	Remember
1.iii.	Define Moore's law. State various IC technologies on the basis of transistor count.	2	2	C314.2	Remember
1.iv.	Explain sheet resistance of a MOS device.	2	2	C314.2	Remember
1.v.	Design a simple NMOS NAND gate	2	1	C314.1	Remember
2.a. b.	Discuss about alternative forms of pull ups Explain the operation of BiCMOS inverter.	5 5	1 1	C314.1 C314.1	Remember Understand
3.	Describe the fabrication process of NMOS with neat sketches.	10	1	C314.1	Understand
4.a. b.	Discuss about NMOS design style Explain in detail rise time and fall time estimation of CMOS inverter delay	5 5	2 2	C314.2 C314.2	Remember Understand
5a. b	. What do you mean by inverter delay? Explain Discuss in detail VLSI design flow.	5 5	2 2	C314.3 C314.3	Understand Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID II Examinations(20-21)
Branch: ECE

SET 1

Sub: VLSI Design (15A04604) **Date: 18-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Draw the circuit of two input NAND gate using CMOS logic.	2	3	C314.3	Apply
1.ii.	What is transmission gate?	2	3	C314.3	Remember
1.iii.	Differentiate DRAMs from SRAMs.	2	4	C314.4	Remember
1.iv.	What is CPLD?	2	4	C314.4	Remember
1.v.	Mention the common techniques involved in ad hoc testing?.	2	5	C314.5	Remember
2.	What are the alternate gate circuits are available, explain them with suitable sketch?	10	3	C314.4	Understand
3.	Discuss about the floor planning..	10	4	C314.5	Understand
4.	What is meant by synthesis? Explain VHDL synthesis.	10	5	C314.6	Understand
5.	a. Draw and explain the architecture of a CPLD. b. Differentiate between the Full-custom and Semi-custom design.	5 5	4 4	C314.4 C314.4	Understand Remember

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID II Examinations(20-21)
Branch: ECE

SET 1

Sub: VLSI Design (15A04604) **Date: 18-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Draw the circuit of two input NAND gate using CMOS logic.	2	3	C314.3	Apply
1.ii.	What is transmission gate?	2	3	C314.3	Remember
1.iii.	Differentiate DRAMs from SRAMs.	2	4	C314.4	Remember
1.iv.	What is CPLD?	2	4	C314.4	Remember
1.v.	Mention the common techniques involved in ad hoc testing?.	2	5	C314.5	Remember
2.	What are the alternate gate circuits are available, explain them with suitable sketch?	10	3	C314.4	Understand
3.	Discuss about the floor planning..	10	4	C314.5	Understand
4.	What is meant by synthesis? Explain VHDL synthesis.	10	5	C314.6	Understand
5.	a. Draw and explain the architecture of a CPLD. b. Differentiate between the Full-custom and Semi-custom design.	5 5	4 4	C314.4 C314.4	Understand Remember

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL

SET 2

B.Tech – III-II Semester (R15) MID II Examinations(20-21)

Branch: ECE

Sub: VLSI Design (15A04604) **Date: 18-8-2021**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Implement the function Y=$\overline{AB+CD}$ with the use of CMOS.	2	3	C314.3	Apply
1.ii.	What is meant by floor planning?.	2	3	C314.3	Remember
1.iii.	Design a simple logic for memory element	2	4	C314.4	Remember
1.iv.	Give the different types of ASIC.	2	4	C314.4	Remember
1.v.	Give some of the important CAD tools	2	5	C314.5	Remember
2.a.	Explain the alternate gate circuits a.Clocked CMOS logic b.N-P CMOS logic	5	3	C314.3	Understand
b.	In detail explain switch logic and its arrangements.	5	3	C314.3	Understand
3.a.	Draw and explain the architecture of FPGA	5	4	C314.4	Understand
b.	Explain semicustom and full custom design	5	4		Understand
4.	Explain in detail design capture and verification tools.	10	5	C314.5	Understand
5.	Draw and explain the architecture of CPLD.	10	4	C314.5	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL

SET 2

B.Tech – III-II Semester (R15) MID II Examinations(20-21)

Branch: ECE

Sub: VLSI Design (15A04604) **Date: 18-8-2021**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Implement the function Y=$\overline{AB+CD}$ with the use of CMOS.	2	3	C314.3	Apply
1.ii.	What is meant by floor planning?.	2	3	C314.3	Remember
1.iii.	Design a simple logic for memory element	2	4	C314.4	Remember
1.iv.	Give the different types of ASIC.	2	4	C314.4	Remember
1.v.	Give some of the important CAD tools	2	5	C314.5	Remember
2.a.	Explain the alternate gate circuits a.Clocked CMOS logic b.N-P CMOS logic	5	3	C314.3	Understand
b.	In detail explain switch logic and its arrangements.	5	3	C314.3	Understand
3.a.	Draw and explain the architecture of FPGA	5	4	C314.4	Understand
b.	Explain semicustom and full custom design	5	4		Understand
4.	Explain in detail design capture and verification tools.	10	5	C314.5	Understand
5.	Draw and explain the architecture of CPLD.	10	4	C314.5	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech III-IISemester (R15) MID II Examinations(20-21)
Branch: ECE

SET 3

Sub: VLSI Design (15A04604) **Date: 18-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	List out various CMOS logic structures?	2	3	C314.3	Remember
1.ii.	What are complementary ways to improve clock distribution	2	3	C314.3	Apply
1.iii.	Explain the working of a magnitude comparator	2	4	C314.4	Remember
1.iv.	Differentiate between channeled and channel less gate array	2	4	C314.4	Remember
1.v.	What are the approaches in design for testability	2	5	C314.5	Remember
2.	What are the alternate gate circuits are available, explain them with suitable sketch?	10	3	C314.3	Understand
3.	Implement arithmetic logic unit to perform both arithmetic and logic functions using full adder and draw the structure of ALU.	10	4	C314.5	Apply
4.	Write a short note on the following tools: (a) Design capture tools. (b) Design verification tools.	10	5	C314.5	Remember
5.a. b.	Compare CPLD and FPGA. Draw the stick diagram of parity generator.	5 5	4 4	C314.4 C314.4	Understand

---

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech III-IISemester (R15) MID II Examinations(20-21)
Branch: ECE

SET 3

Sub: VLSI Design (15A04604) **Date: 18-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	List out various CMOS logic structures?	2	3	C314.3	Remember
1.ii.	What are complementary ways to improve clock distribution	2	3	C314.3	Apply
1.iii.	Explain the working of a magnitude comparator	2	4	C314.4	Remember
1.iv.	Differentiate between channeled and channel less gate array	2	4	C314.4	Remember
1.v.	What are the approaches in design for testability	2	5	C314.5	Remember
2.	What are the alternate gate circuits are available, explain them with suitable sketch?	10	3	C314.3	Understand
3.	Implement arithmetic logic unit to perform both arithmetic and logic functions using full adder and draw the structure of ALU.	10	4	C314.5	Apply
4.	Write a short note on the following tools: (a) Design capture tools. (b) Design verification tools.	10	5	C314.5	Remember
5.a. b.	Compare CPLD and FPGA. Draw the stick diagram of parity generator.	5 5	4 4	C314.4 C314.4	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL

SET 4

B.Tech – III-II Semester (R15) MID II Examinations(20-21)
Branch: ECE

Sub: VLSI Design (15A04604) **Date: 18-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Write the features of CMOS Domino Logic?	2	3	C314.3	Apply
1.ii.	Write short notes on switch logic.	2	3	C314.3	Remember
1.iii.	What is FPGA?	2	4	C314.4	Remember
1.iv.	What is built -in -self -test?	2	5	C314.5	Remember
1.v.	What are the different types of modelling in VHDL?	2	5	C314.5	Remember
2.	Write short notes about the following a. CMOS logic b.Pseudo NMOS c. Dynamic CMOS logic d.Domino CMOS logic	10	3	C314.4	Understand
3.a. b.	Write the differences between SRAM and DRAM. In detail explain switch logic and its arrangements.	5 5	4 3	C314.4 C314.3	Understand Understand
4.	What is meant by simulation. Explain in detail the various VHDL simulations.	10	5	C314.5	Understand
5.	Draw and explain the architecture of CPLD	10	4	C314.4	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL

SET 4

B.Tech – III-II Semester (R15) MID II Examinations(20-21)
Branch: ECE

Sub: VLSI Design (15A04604) **Date: 18-8-2021**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Write the features of CMOS Domino Logic?	2	3	C314.3	Apply
1.ii.	Write short notes on switch logic.	2	3	C314.3	Remember
1.iii.	What is FPGA?	2	4	C314.4	Remember
1.iv.	What is built -in -self -test?	2	5	C314.5	Remember
1.v.	What are the different types of modelling in VHDL?	2	5	C314.5	Remember
2.	Write short notes about the following a. CMOS logic b.Pseudo NMOS c. Dynamic CMOS logic d.Domino CMOS logic	10	3	C314.4	Understand
3.a. b.	Write the differences between SRAM and DRAM. In detail explain switch logic and its arrangements.	5 5	4 3	C314.4 C314.3	Understand Understand
4.	What is meant by simulation. Explain in detail the various VHDL simulations.	10	5	C314.5	Understand
5.	Draw and explain the architecture of CPLD	10	4	C314.4	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations(19-20)
Branch: ECE

SET 1

Sub: VLSI Design (15A04604) **Date: 11-3-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Define Moore's law. State various IC technologies on the basis of transistor count.	2	1	C314.1	Remember
1.ii.	Differentiate between PMOS and NMOS transistors.	2	1	C314.1	Analyze
1.iii.	Write about latch up and mention the remedy process to reduce it.	2	2	C314.2	Remember
1.iv.	Discuss the scaling factors for the device parameter Current density and gate capacitance.	2	2	C314.3	Remember
1.v.	Design a simple NMOS NOR gate.	2	1	C314.3	Apply
2.	Draw V-I characteristics of NMOS transistor. Explain its operation.Derive the drain to source current equation in saturation and resistive region.	10	1	C314.2	Understand
3.a b.	Explain in detail the operation of nMOS inverter and draw its transfer characteristics. An N- MOSFET has Vt of 0.8 V,gate voltage of 3.5V and drain voltage of 2.5V, source voltage of 0.5V.Find the region of operation of MOSFET .	7 3	1	C314.1	Understand Apply
4.a. b.	Write about fan in and fan out and draw the characteristics. Calculate the inverter delay through a pair of nMOS and CMOS inverters.	2 8	2	C314.2	Apply
5.	Define stick diagram. Draw a stick diagram for two input NMOS $Y=(AB+CD+EF)^1$ and CMOS EXOR gate.	10	2	C314.3	Apply

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations(19-20)
Branch: ECE

SET 2

Sub: VLSI Design (15A04604) **Date: 11-3-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Describe the operating regions for a MOS transistor.	2	1	C314.1	Remember
1.ii.	Explain pass transistor logic and draw the symbol of transmission gate.	2	1	C314.2	Understand
1.iii.	What is channel length modulation?	2	1	C314.2	Remember
1.iv.	Explain sheet resistance of a MOS device.	2	2	C314.3	Remember
1.v.	Draw a two iput NAND gate using nMOS logic.	2	2	C314.3	Remember
2.a. b.	Compare NMOS and PMOS transistors. Explain NMOS fabrication process with neat diagrams.	2 8	1	C314.1	Analyze Understand
3.	Design a CMOS inverter circuit and explain about its various regions of operation in detail with the necessary diagrams.	10	1	C314.2	Apply
4.a. b.	Write about design rules for wires(NMOS and CMOS) Draw the stick diagram and layout diagram for NOT gate in CMOS design style.	2 8	2	C314.3	Understand
5.	Define delay unit and prove that rise time is 2.5 times of fall time and risetime proportional to C_L.	10	2	C314.2	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations((19-20)
Branch: ECE

SET 3

Sub: VLSI Design (15A04604) **Date: 11-3-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Derive an expression for transconductance.	2	1	C314.1	Analyze
1.ii.	An n-MOSFET has threshold voltage of 1v, gate voltage of 2v and drain voltage of 2.5v.Find the region of operation of the MOSFET.	2	1	C314.2	Apply
1.iii.	Define stick diagram and design process.	2	2	C314.3	Remembre
1.iv.	Discuss the scaling factors for the device parameters. Channel resistance and gate delay.	2	2	C314.2	Remember
1.v.	Draw the logical circuit of two input CMOS EXOR gate.	2	2	C314.3	Remember
2.a. b.	Explain in detail the enhancement mode transistor action wih neat diagrams. List the advantages of CMOS technology.	8 2	1	C314.1	Understand, Remember
3.	Determine the pull-up to pull down ratio of an nMOS inverter driven by pass transistor.	10	1	C314.2	Understand
4.a. b.	Mention the design rules for contact cuts and transistors. Draw a stick diagram for two input nMOS NAND and CMOS NOR gates.	3 7	2	C314.3	Remember, Understand
5.a. b.	Define delay unit. Two CMOS inverters are cascaded to drive a load capacitor $C_L=25C_g$.Calculate the pair delay in terms of τ. Explain how super buffers are used to drive large capacitive loads.	5 5	2	C314.2	Apply, Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations(19-20)
Branch: ECE

SET 4

Sub: VLSI Design (15A04604) **Date: 11-3-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Define speed power product.	2	1	C314.2	Remember
1.ii.	Distinguish between CMOS and Bipolar.	2	1	C314.1	Remember
1.iii.	Calculate the standard of value of gate capacitance for 5µm technology.	2	2	C314.2	Remember
1.iv.	Explain sheet resistance of a MOS device.	2	2	C314.2	Remember
1.v.	A n- MOSFET has Vt of 0.6 V,gate voltage of 1.5V and drain voltage of 3V.Find the region of operation of MOSFET .	2	1	C314.1	Remember
2.a. b.	Illustrate the steps involved in P-well CMOS fabrication process and draw the flow chart. Explain the operation of BiCMOS inverter.	7 3	1	C314.1	Remember Understand
3.	Determine the pull-up to pull down ratio of an nMOS inverter driven by another NMOS inverter.	10	1	C314.2	Understand
4.a. b.	Mention the design rules to draw CMOS stick diagrams. Draw the stick diagram for Y= ((A+B)(C+D)) using CMOS logic and NMOS NOR gate.	2 8	2	C314.3	Remember Apply
5a. b	What is scaling.Explain substrate doping,limits of miniaturization. Discuss in detail VLSI design flow.	3 7	2	C314.3	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL

B.Tech: III-II Semester MID II Examinations 2019-20

Branch: ECE

SET-I

Sub: VLSI Design **Date:11-11-2020**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Draw the circuit of two input NAND gate using CMOS logic.	2	3	C314.3	Apply
1.ii.	What is transmission gate?	2	3	C314.3	Remember
1.iii.	Differentiate DRAMs from SRAMs.	2	4	C314.4	Remember
1.iv.	What is CPLD?	2	4	C314.4	Remember
1.v.	Mention the common techniques involved in ad hoc testing?.	2	5	C314.5	Remember
2.	What are the alternate gate circuits are available, explain them with suitable sketch?	10	3	C314.4	Understand
3.	Discuss about the floor planning..	10	4	C314.5	Understand
4.	What is meant by synthesis? Explain VHDL synthesis.	10	5	C314.6	Understand
5.	a. Draw and explain the architecture of a CPLD. b. Differentiate between the Full-custom and Semi-custom design.	5 5	4 4	C314.4 C314.4	Understand Remember

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL

B.Tech: III-II Semester MID II Examinations 2019-20

Branch: ECE

SET-II

Sub: VLSI Design **Date:11-11-2020**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Implement the function Y=$\overline{AB+CD}$ with the use of CMOS.	2	3	C314.3	Apply
1.ii.	What is meant by floor planning?.	2	3	C314.3	Remember
1.iii.	Design a simple logic for memory element	2	4	C314.4	Remember
1.iv.	Give the different types of ASIC.	2	4	C314.4	Remember
1.v.	Give some of the important CAD tools	2	5	C314.5	Remember
2.a.	Explain the alternate gate circuits a.Clocked CMOS logic b.N-P CMOS logic	5	3	C314.3	Understand
b.	In detail explain switch logic and its arrangements.	5	3	C314.3	Understand
3.a.	Draw and explain the architecture of FPGA	5	4	C314.4	Understand
b.	Explain semicustom and full custom design	5	4		Understand
4.	Explain in detail design capture and verification tools.	10	5	C314.5	Understand
5.	Draw and explain the architecture of CPLD.	10	4	C314.5	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL
B.Tech: III-II Semester MID II Examinations 2019-20
Branch: ECE

SET-III

Sub: VLSI Design **Date:11-11-2020**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	List out various CMOS logic structures?	2	3	C314.3	Remember
1.ii.	What are complementary ways to improve clock distribution	2	3	C314.3	Apply
1.iii.	Explain the working of a magnitude comparator	2	4	C314.4	Remember
1.iv.	Differentiate between channeled and channel less gate array	2	4	C314.4	Remember
1.v.	What are the approaches in design for testability	2	5	C314.5	Remember
2.	What are the alternate gate circuits are available, explain them with suitable sketch?	10	3	C314.3	Understand
3.	Implement arithmetic logic unit to perform both arithmetic and logic functions using full adder and draw the structure of ALU.	10	4	C314.5	Apply
4.	Write a short note on the following tools: (a) Design capture tools. (b) Design verification tools.	10	5	C314.5	Remember
5.a. b.	Compare CPLD and FPGA. Draw the stick diagram of parity generator.	5 5	4 4	C314.4 C314.4	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL

B.Tech: III-II Semester MID II Examinations 2019-20

SET-IV

Branch: ECE

Sub: VLSI Design **Date:11-11-2020**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Write the features of CMOS Domino Logic?	2	3	C314.3	Apply
1.ii.	Write short notes on switch logic.	2	3	C314.3	Remember
1.iii.	What is FPGA?	2	4	C314.4	Remember
1.iv.	What is built -in -self -test?	2	5	C314.5	Remember
1.v.	What are the different types of modelling in VHDL?	2	5	C314.5	Remember
2.	Write short notes about the following a. CMOS logic b.Pseudo NMOS c. Dynamic CMOS logic d.Domino CMOS logic	10	3	C314.4	Understand
3.a. b.	Write the differences between SRAM and DRAM. In detail explain switch logic and its arrangements.	5 5	4 3	C314.4 C314.3	Understand Understand
4.	What is meant by simulation. Explain in detail the various VHDL simulations.	10	5	C314.5	Understand
5.	Draw and explain the architecture of CPLD	10	4	C314.4	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations(18-19)
Branch: ECE

SET 2

Sub: VLSI Design (15A04604) **Date: 11-5-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Define Moore's law. State various IC technologies on the basis of transistor count.	2	1	C314.1	Remember
1.ii.	Differentiate between PMOS and NMOS transistors.	2	1	C314.1	Analyze
1.iii.	Write about latch up and mention the remedy process to reduce it.	2	2	C314.2	Remember
1.iv.	Discuss the scaling factors for the device parameter Current density and gate capacitance.	2	2	C314.3	Remember
1.v.	Design a simple NMOS NOR gate.	2	1	C314.3	Apply
2.	Draw V-I characteristics of NMOS transistor. Explain its operation.Derive the drain to source current equation in saturation and resistive region.	10	1	C314.2	Understand
3.a b.	Explain in detail the operation of nMOS inverter and draw its transfer characteristics. An N- MOSFET has Vt of 0.8 V,gate voltage of 3.5V and drain voltage of 2.5V, source voltage of 0.5V.Find the region of operation of MOSFET .	7 3	1	C314.1	Understand Apply
4.a. b.	Write about fan in and fan out and draw the characteristics. Calculate the inverter delay through a pair of nMOS and CMOS inverters.	2 8	2	C314.2	Apply
5.	Define stick diagram. Draw a stick diagram for two input NMOS $Y=(AB+CD+EF)^1$ and CMOS EXOR gate.	10	2	C314.3	Apply

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations(18-19
Branch: ECE

SET 1

Sub: VLSI Design (15A04604) **Date: 11-5-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Describe the operating regions for a MOS transistor.	2	1	C314.1	Remember
1.ii.	Explain pass transistor logic and draw the symbol of transmission gate.	2	1	C314.2	Understand
1.iii.	What is channel length modulation?	2	1	C314.2	Remember
1.iv.	Explain sheet resistance of a MOS device.	2	2	C314.3	Remember
1.v.	Draw a two iput NAND gate using nMOS logic.	2	2	C314.3	Remember
2.a. b.	Compare NMOS and PMOS transistors. Explain NMOS fabrication process with neat diagrams.	2 8	1	C314.1	Analyze Understand
3.	Design a CMOS inverter circuit and explain about its various regions of operation in detail with the necessary diagrams.	10	1	C314.2	Apply
4.a. b.	Write about design rules for wires(NMOS and CMOS) Draw the stick diagram and layout diagram for NOT gate in CMOS design style.	2 8	2	C314.3	Understand
5.	Define delay unit and prove that rise time is 2.5 times of fall time and risetime proportional to C_L.	10	2	C314.2	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations((18-19
Branch: ECE

SET 4

Sub: VLSI Design (15A04604) **Date: 11-5-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Derive an expression for transconductance.	2	1	C314.1	Analyze
1.ii.	An n-MOSFET has threshold voltage of 1v, gate voltage of 2v and drain voltage of 2.5v.Find the region of operation of the MOSFET.	2	1	C314.2	Apply
1.iii.	Define stick diagram and design process.	2	2	C314.3	Remembre
1.iv.	Discuss the scaling factors for the device parameters. Channel resistance and gate delay.	2	2	C314.2	Remember
1.v.	Draw the logical circuit of two input CMOS EXOR gate.	2	2	C314.3	Remember
2.a. b.	Explain in detail the enhancement mode transistor action wih neat diagrams. List the advantages of CMOS technology.	8 2	1	C314.1	Understand, Remember
3.	Determine the pull-up to pull down ratio of an nMOS inverter driven by pass transistor.	10	1	C314.2	Understand
4.a. b.	Mention the design rules for contact cuts and transistors. Draw a stick diagram for two input nMOS NAND and CMOS NOR gates.	3 7	2	C314.3	Remember, Understand
5.a. b.	Define delay unit. Two CMOS inverters are cascaded to drive a load capacitor $C_L=25C_g$.Calculate the pair delay in terms of τ. Explain how super buffers are used to drive large capacitive loads.	5 5	2	C314.2	Apply, Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID I Examinations(18-19
Branch: ECE

SET 3

Sub: VLSI Design (15A04604) **Date: 11-5-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Define speed power product.	2	1	C314.2	Remember
1.ii.	Distinguish between CMOS and Bipolar.	2	1	C314.1	Remember
1.iii.	Calculate the standard of value of gate capacitance for 5µm technology.	2	2	C314.2	Remember
1.iv.	Explain sheet resistance of a MOS device.	2	2	C314.2	Remember
1.v.	A n- MOSFET has Vt of 0.6 V,gate voltage of 1.5V and drain voltage of 3V.Find the region of operation of MOSFET .	2	1	C314.1	Remember
2.a. b.	Illustrate the steps involved in P-well CMOS fabrication process and draw the flow chart. Explain the operation of BiCMOS inverter.	7 3	1	C314.1	Remember Understand
3.	Determine the pull-up to pull down ratio of an nMOS inverter driven by another NMOS inverter.	10	1	C314.2	Understand
4.a. b.	Mention the design rules to draw CMOS stick diagrams. Draw the stick diagram for Y= ((A+B)(C+D)) using CMOS logic and NMOS NOR gate.	2 8	2	C314.3	Remember Apply
5a. b	What is scaling.Explain substrate doping,limits of miniaturization. Discuss in detail VLSI design flow.	3 7	2	C314.3	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech – III-II Semester (R15) MID II Examinations(18-19)
Branch: ECE

SET 1

Sub: VLSI Design (15A04604) **Date: 10-5-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Draw the circuit of two input EXOR gate using CMOS logic.	2	3	C314.4	Apply
1.ii.	Define modularity.	2	5	C314.4	Remember
1.iii.	List the advantages of simulation.	2	5	C314.5	Remember
1.iv.	What is placement? Write about different levels of placement.	2	4	C314.6	Remember
1.v.	Mention thedifferences between SRAM and DRAM.	2	4	C314.6	Remember
2.	Mention the advantages of dynamic logic structures over static logic and explain various alternate gate circuits.	10	3	C314.4	Understand
3.	Draw and explain the FPGA architecture.	10	4	C314.5	Understand
4.	What is meant by synthesis? Explain VHDL synthesis.	10	5	C314.6	Understand
5.	a.Discuss about the floor planning. b.Explain the working of magnitude comparator.	7 3	3 4	C314.5	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL

B.Tech – III-II Semester (R15) MID II Examinations(18-19)

Branch: ECE

SET 2

Sub: VLSI Design (15A04604) **Date: 10-5-2019**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Draw the circuit symbol of two input CMOS EXNOR gate.	2	3	C314.4	Apply
1.ii.	Define the terms simulation and synthesis.	2	3	C314.6	Remember
1.iii.	Write short notes on channeled gate arrays.	2	4	C314.5	Remember
1.iv.	Mention the classification of ASICs.	2	5	C314.5	Remember
1.v.	Write short notes on different types of errors in simulation.	2	5	C314.6	Remember
2.a. b.	Explain the alternate gate circuits a.Clocked CMOS logic b.N-P CMOS logic In detail explain switch logic and its arrangements.	6 4	3	C314.4	Understand
3.a. b.	Discuss in detail the two phase clocking circuitary. Explain semicustom and full custom design	6 4	3 4	C314.4	Understand
4.	Mention the objectives of BIST and explain different BIST techniques.	10	5	C314.6	Understand
5.	Draw and explain the architecture of CPLD.	10	4	C314.5	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
B.Tech III-IISemester (R15) MID II Examinations(18-19)
Branch: ECE

SET 3

Sub: VLSI Design (15A04604) **Date: 10-5-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Define regularity.	2	3	C314.4	Remember
1.ii.	Draw the symbol of tansmission gate and explain.	2	3	C314.4	Apply
1.iii.	Compare CPLD and FPGA.	2	4	C314.5	Remember
1.iv.	List the advantages and applications of FPGA.	2	4	C314.6	Remember
1.v.	Explain controllability.	2	5	C314.6	Remember
2.a. b.	Discuss about the different levels of placement. Explain VLSI design flow.	8 2	3	C314.4	Understand
3.	Implement arithmetic logic unit to perform both arithmetic and logic functions using full adder and draw the structure of ALU.	10	4	C314.5	Apply
4.	Explain various design capture and verification tools.	10	5	C314.6	Remember
5.a. b.	Explain the working of 1T and 3T DRAM cell. Draw the stick diagram of parity generator.	8 2	4	C314.5	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN:KURNOOL
L
B.Tech – III-II Semester (R15) MID II Examinations(18-19)
Branch: ECE

SET 4

Sub: VLSI Design (15A04604) **Date:10-5-2019**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 ,one from 4 or 5 .

S.no	Questions	Marks	Unit	CO	Cognitive Level
1.i.	Draw the logic circuit of two input CMOS EXNOR gate.	2	3	C314.4	Apply
1.ii.	Write short notes on switch logic.	2	3	C314.4	Remember
1.iii.	Compare FPGA and CPLD.	2	4	C314.5	Remember
1.iv.	Define hierarchy.	2	5	C314.6	Remember
1.v.	List the objectives of BIST.	2	5	C314.6	Remember
2.a	Write short notes about the following a. CMOS logic b.Pseudo NMOS c. Dynamic CMOS logic d.Domino CMOS logic	10	3	C314.4	Understand
3.a. b.	Write the differences between SRAM and DRAM. Mention the disadvantages of 4T SRAM and explain the working of 6T SRAM with necessary diagrams.	2 8	4	C314.5	Understand
4.	What is meant by simulation. Explain in detail the various VHDL simulations.	10	5	C314.6	Understand
5.a b	Draw the stick diagram of parity generator and explain in detail. Explain the working of pass transistor logic.	8 2	4	C314.5	Understand