

**JNTUA UNIVERSITY  
PREVIOUS QUESTION PAPERS**

## B.Tech II Year - II Semester Examinations, April-May, 2012

## SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, ETM, BME)

Time: 3 hours

Max. Marks: 75

Answer any five questions

All questions carry equal marks

- 1.a) Convert the number  $(17.125)_{16}$  to base 10, base 4, base 5 and base 2.  
 b) Perform the binary arithmetic operations on  $(-14)_{10} - (-2)_{10}$  using signed 2's complement representation.  
 c) Justify the statement that "Gray code is a class of reflected code". [6+6+3]
- 2.a) State and Prove De Morgan's theorem of Boolean Algebra.  
 b) Determine the canonical product-of-sums and sum-of-products form of  $T(x,y,z) = x'(y' + z')$   
 c) Realize the basic gates using NAND and NOR gates only. [5+ 4+6]
- 3.a) Prove that if  $w'x + yz' = 0$ , then  $wx + y'(w' + z') = wx + xz + x'z' + w'y'z$ .  
 b) For the given function  $T(w,x,y,z) = \Sigma (0,1,2,3,4,6,7,8,9,11,15)$   
 i) Show the map  
 ii) Find all prime implicants and indicate which are essential.  
 iii) Find a minimal expression for T and realize using basic gates. Is it unique?  
 [7+8]
- 4.a) Design a 2-bit comparator which compares the magnitude of two numbers X and Y and generates three output  $f_1, f_2$ , and  $f_3$ .  
 b) Realize  $16 \times 1$  Mux using only  $2 \times 1$  Mux. [8+7]
- 5.a) Realize the given function using PLD circuit  $F(x,y,z) = xy + yz + x'y'$ .  
 b) What is meant by Logic simulation, Functional simulation, timing simulation and Logic synthesis? [9+6]
- 6.a) Design a BCD counter using JK Flip-Flops.  
 b) Write the differences between synchronous and asynchronous counters.  
 c) Draw the state diagram and characteristic table of Master Slave JK flip-flop.  
 [8+3+4]
- 7.a) Write the differences between completely specified function and incompletely specified functions with examples.

- b) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 0, input X is transferred to Z, otherwise, the output remains same. [6+9]
- 8.a) Differentiate between Mealy and Moore machine with examples.
- b) Write about the implementation of Binary multiplier. [8+7]

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All questions carry equal marks

- 1.a) Convert the number  $(127.75)_8$  to base 10, base 3, base 16 and base 2.
- b) Given that  $(64)_{10} = (100)_b$ , determine the value of b.
- c) Perform the binary arithmetic operations on  $(+12) - (4)$  using signed 2's complement representation. [5+4+6]
- 2.a) State and Prove the Huntington postulates of Boolean Algebra.
- b) Find the complement of the function and represent in sum of minterms  
 $F(x,y,z) = xy + z'$
- c) Simplify the following function and realize using universal gates  
 $F(A,B,C) = A'BC' + ABC + B'C' + A'B'$  [5+4+6]
- 3.a) Use the tabulation procedure to generate the set of prime implicants and to obtain all minimal expressions for the following function  
 $F(a,b,c,d) = \Sigma (1,5,6,12,13,14) + \Sigma d(2,4)$
- b) For the given function  $T(w,x,y,z) = \Sigma (0,1,5,7,8,10,14,15)$ 
  - i) Show the map
  - ii) Find all prime implicants and indicate which are essential.
  - iii) Find a minimal expression and realize using basic gates. [8+7]
- 4.a) Design a combinational circuit to find the 2's complement of a given 4bit binary number and realize using NAND gates.
- b) Design a full adder using Multiplexer. [8+7]
- 5.a) What is PAL? How does it differ from PROM and PLA?
- b) Design a switching circuit that converts a 4 bit binary code into a 4 bit Gray code using ROM array. [6+9]
- 6.a) Define Setup and Hold times.
- b) Write the characteristic, excitation tables for JK, RS, T and D flip-flops.
- c) Design a synchronous counter to generate the sequence 0,1,1,2,3,5,8, and repeat the sequence using T flip-flops. [2+6+7]

- 7.a) Construct the state diagram and primitive flow table for an asynchronous Machine that has two inputs and one output. The input sequence  $xy = 00, 01, 10$  Causes the output to become 1. The next input change then causes the output to return to 0. No other inputs will produce a 1 output.
- b) Write the usage of merger graph with example. [8+7]
- 8.a) Write the usage of Mealy machine with example.
- b) Discuss the implementation of Binary multiplier with appropriate realizations. [8+7]

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## SWITCHING THEORY AND LOGIC DESIGN

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Answer any five questions

All questions carry equal marks

- 1.a) Convert the following to the required form.  
 i)  $(A98B)_{12} = (\text{-----})_3$  ii)  $(38.65)_{10} = (\text{-----})_2$ .
- b) Use 2's complement form perform subtraction.  
 i)  $1101010 - 110100$  ii)  $10011.1101 - 101.11$  [15]
- 2.a) Simplify the following  
 i)  $(A + AC + B)$  ii)  $F = AB(C + C) + AB$  iii)  $F = (X + Y)(X + Z)$
- b) Prove that NAND and NOR gates are Universal gates. [15]
- 3.a) Simplify the following function using K-map.  
 $F(A,B,C,D) = \Sigma(1,3,4,5,6,11,13,14,15)$
- b) Simplify the following using Tabular method.  
 $F(A,B,C,D) = \Sigma(3,7,8,12,13,15) + (9,14) \phi \Sigma$ . [15]
- 4.a) Design a 64:1 MUX using 8:1 MUXs.  
 b) Design a 4 bit parallel adder using Full adder modules. [15]
- 5.a) Design a 4-bit parity checker/ generator circuit that can generate even parity using logic gates.  
 b) Write a brief note on threshold logic synthesis. [15]
- 6.a) What is meant by clock skew? How to handle it?  
 b) Explain the term Race around condition. How is it satisfied by Master-slave Flip-Flops. [15]
- 7.a) Design a modulo 10 counter JK flipflops.  
 b) What are the rules to develop a Merger chart? [15]
8. Design a binary multiplier and its control logic by drawing ASM chart and realize the same using decoder, MUX and D flipflops. [15]

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## SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, ETM, BME)

Time: 3 hours

Max. Marks: 75

Answer any five questions

All questions carry equal marks

- 1.a) Develop a Gray code for  $(42)_{10}$  and  $(97)_{10}$  and convert the same to Hex sequence.
- b) Explain different error detecting and correcting codes in digital system. [15]
- 2.a) Show that i)  $AB + \bar{A}B = A \oplus B$   
 ii)  $(A \oplus B) = (A \oplus B)$
- b) Reduce the following boolean expressions using theorems and identities.
- i)  $F = C + AB + AD(B + C) + CD$   
 ii)  $F = AB + CDB + ACD$  [15]
- 3.a) Simplify the following using prime implicant chart method.  
 $f(A,B,C,D) = \Sigma(0,5,7,8,9,10,11,13)$
- b) Use tabular method and simplify the following 5 variable function  
 $F(A,B,C,D,E) = \Sigma(0,4,8,12,16,20,24,28) + \Sigma\phi(1,5,7,23)$ . [15]
- 4.a) Design a 4 bit comparator circuit using logic gates.
- b) Design a code converter logic circuit which converts BCD code to Excess-3 code. [15]
- 5.a) Design a square generator logic for 4 bit input using ROM.
- b) What are the capabilities and limitations of threshold gate? [15]
- 6.a) Convert RS flip flop to a  
 i) D-latch ii) T-latch.
- b) Design a FSM which detects 0011 pattern and set  $z = 1$  for all other patterns  $z = 0$  [15]
- 7.a) Design a multi mode universal shift registers of 4 bit.
- b) Draw a block diagram of Modulo 10 ripple counter and explain its timing diagram. [15]
8. Design a control logic through ASM Chart for the sequence detector which detects 1100 and resets flip flop F to 0 and flip flop E to 1. The patterns come from 4 bit counter A. [15]

B.Tech II Year I Semester (R13) Supplementary Examinations November/December 2016

**SWITCHING THEORY & LOGIC DESIGN**

(Common to ECE and EIE)

Time: 3 hours

Max. Marks: 70

**PART – A**

(Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- What is the decimal equivalent of hexadecimal number 1A53?
  - Simplify the following Boolean expression:  $(A'BC')' + (AB'C)'$ .
  - Simplify the following function using K- map:  $F(x, y, z) = \Sigma(2, 3, 4, 5)$ .
  - Construct a logic circuit using NAND gates only for the expression  $x = A.(B + C)$ .
  - What do you understand by Combinational logic circuits? Give example.
  - What is multiplexer? Draw the block diagram of 4-input MUX.
  - What is the difference between latch and flip flop?
  - What is shift register? List out some applications of Shift Register.
  - How race around condition can be eliminated?
  - What are hazards in digital logic circuits? How they can be resolved?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 Simplify the following identities using Boolean algebra:

(a)  $(A+B)(A+(AB)')C+A'(B+C')+A'B+ABC$ .

(b)  $\overline{\overline{A(A \cdot B)} \cdot \overline{B(A \cdot B)}}$

**OR**

- 3 (a) Simplify and draw the logic diagram for the given expression:  
 $F = (ABC)' + (AB)'C + A'BC' + A(BC)' + AB'C$
- (b) Simplify the expressions using Boolean postulates:  $F = XY + (XZ)' + XY'Z (XY + Z)$ .

**UNIT – II**

- 4 (a) Simplify the following expression using the K-map:  $Y = A'B'C' + AC'D' + AB' + ABCD' + A'B'C$
- (b) Write the expression for Boolean function  $F(A, B, C) = \Sigma m(1, 4, 5, 6, 7)$  in standard POS form.

**OR**

- 5 Simplify the following expression to sum of products using Tabulation Method:  
 $F(a, b, c, d) = \Sigma m(0, 4, 8, 10, 12, 13, 15) + d(1, 2)$

**UNIT – III**

- 6 Discuss in detail, the working of full adder logic circuit and extend your discussion to explain a binary adder, which can be used to add two binary numbers.

**OR**

- 7 (a) Draw the logic circuit of a 3 to 8 decoder and explain its working.
- (b) Explain the working of a De-multiplexer with the help of an example.

**UNIT – IV**

- 8 Using D-Flip flops and waveforms, explain the working of a 4-bit SISO shift register.

**OR**

- 9 With the help of clocked JK flip flops and waveforms, explain the working of a 3-bit binary ripple counter. Write truth table for clock transitions.

**UNIT – V**

- 10 Difference between static and dynamic RAM. Draw the circuits of one cell of each and explain its working.

**OR**

- 11 Is the ROM a volatile memory? Explain. Also draw the logic diagram of 16-bit ROM Array and explain its principle of operation.

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**SWITCHING THEORY & LOGIC DESIGN**

(Common to EEE and ECE)

Time: 3 hours

Max. Marks: 70

**PART – A**

(Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- State and Prove consensus theorem.
  - Find the 2's complement of representation of -9.
  - Design a XOR gate using minimum number of NAND gates.
  - Find the minimum number of literals for the following function using 2 variable Karnaugh Map.  
 $F = \sum m(1) + d(3)$ . d - Don't care.
  - Write the sum and carry expression for half adder.
  - Implement the function  $F = \sum m(0, 2)$  using a  $2 \times 4$  decoder.
  - Write the characteristic equation for JK Flip-flop.
  - How many states are there in a n-bit ring counter?
  - Compare PROM & PAL.
  - What is meant by cycle in asynchronous circuits?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 (a) Express the following function  $F = xy + x'y$  in a product of max-terms.  
 (b) Check if NOR gate is associative or not.

**OR**

- 3 (a) Show that a positive logic NAND gate is a negative logic OR gate  
 (b) Obtain the truth table of the following function and express in sum of min-terms and product of max-terms:  $F = (A' + B).(B' + C)$ .

**UNIT – II**

- 4 Simplify the Boolean function using K map technique:  
 (a)  $F = \pi M(3, 4, 6, 7, 11, 12, 13, 14, 15)$ .  
 (b)  $F = \sum m(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$ .

**OR**

- 5 Simplify the following Boolean function using tabulation method:  
 $F = \sum m(0, 1, 2, 3, 5, 7, 8, 10, 14, 15)$ .

**UNIT – III**

- 6 Design a 4-Bit Magnitude comparator using logic gates.

**OR**

- 7 (a) Implement the function  $F = \sum m(0, 1, 2, 4, 5, 8, 11, 12, 15)$  using 8:1 multiplexer.  
 (b) Design a half subtractor using logic gates.

**UNIT – IV**

- 8 Design a 4 bit universal shift register with neat diagram.

**OR**

- 9 Design a 3 bit synchronous up counter using T Flip-flops.

**UNIT – V**

- 10 Implement the following functions using PLA with three inputs, four product terms and two outputs.  
 $F_1(A, B, C) = \sum m(3, 5, 6, 7)$ ,  $F_2(A, B, C) = \sum m(0, 2, 4, 7)$ .

**OR**

- 11 Implement the switching function  $F = \sum m(1, 3, 5, 7, 8, 9, 14, 15)$  by a static hazard free two level AND-OR network.

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B.Tech II Year I Semester (R13) Regular & Supplementary Examinations December 2015  
**SWITCHING THEORY & LOGIC DESIGN**  
 (Common to ECE and EIE)

Time: 3 hours

Max. Marks: 70

**PART – A**  
 (Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- State and prove De-Morgans theorem.
  - What do you understand by universal gate?
  - Convert the given equation  $Y=AB+AC'+BC$  into standard SOP form.
  - Implement the following Boolean equation using only NAND gates  $Y=AB+CDE+F$ .
  - Draw the logic diagram of full adder circuit and form the truth table.
  - What is multiplier? Draw the block diagram of 4-input MUX.
  - Give the comparison between combinational circuits and sequential circuits.
  - What is shift register? Give the classification of them.
  - What are the steps involved in designing an asynchronous sequential circuits?
  - What are hazards in digital logic circuits? How it can be resolved?

**PART – B**  
 (Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 Simplify the following Boolean expression: (i)  $F = (A+B)(A'+C)(B+C)$ . (ii)  $F = A+B+C'+D(E+F)'$
- OR**
- 3 (a) Expand the following Boolean functions  $F = xy+x'z$  in a standard product of maxterm form.  
 (b) Minimize the following Boolean function:  $f(A,B,C,D)=\sum m(5,7,8,10,13,15)+\sum d(0,1,2,3)$ .

**UNIT – II**

- 4 (a) Simplify the following expression using the K-map for the 4-variable:  
 $Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C'$   
 (b) Implement the following Boolean function using NOR gates  $Y=(AB'+A'B)(C+D)'$ .

**OR**

- 5 Simplify the Boolean function by using tabulation method.  
 $F(a,b,c,d)=\sum m(0,1,2,5,6,7,8,9,10,14)$

**UNIT – III**

- 6 Discuss in detail about the design procedure for binary serial and parallel adder with diagram.
- OR**
- 7 Implement a 2-bit Magnitude comparator and write down its design procedure.

**UNIT – IV**

- 8 A sequential circuit with two D-flip flops A and B, two inputs 'x' and 'y' and one output 'z' is specified by the following next state and output equation.  
 $A(t+1) = x'y+xA$ ,  $B(t+1) = x'B+xA$  and  $Z = B$   
 (i) Draw the logic diagram of the circuit. (ii) List the state table and draw the corresponding state diagram.

**OR**

- 9 Design and implement 3-bit ripple counter using J-K flip flop. Draw the state diagram, logic diagram and timing diagram for the same.

**UNIT – V**

- 10 What is critical and non-critical races in asynchronous circuits? How to avoid races? Illustrate with one example.
- OR**
- 11 Design and implement the following Boolean functions in PAL.
- $A(w,x,y,z)=\sum m(0,2,6,7,8,9,12,13)$
  - $B(w,x,y,z)=\sum m(0,2,6,7,8,9,12,13,14)$
  - $C(w,x,y,z)=\sum m(1,3,4,6,10,12,13)$
  - $D(w,x,y,z)=\sum m(1,3,4,6,9,12,14)$

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**SWITCHING THEORY AND LOGIC DESIGN**

(Common to ECE &amp; EIE)

Time: 3 hours

Max. Marks: 70

**PART - A**

(Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- Find the complement of the function  $F = A + BC$  and show that  $F \cdot \bar{F} = 0$ .
  - Perform the subtraction operation on 22-7 using 2's complement form.
  - Convert the expression  $f(A, B, C) = (A + B)(B + C)(A + C)$  in standard POS form.
  - Simplify  $\overline{AB + A} + AB$ .
  - Obtain the prime implicants for given Boolean expression.  
 $f(A, B, C) = \sum(0, 1, 3, 5, 7)$  using k-map.
  - Design a 4 bit parallel adder using Full adders.
  - Explain how decoder can be converted into a demultiplexer with a neat block diagram.
  - Compare PROM, PLA & PAL.
  - Compare level and edge triggering.
  - Assume that the 5 bit binary counter starts in the 0000 state then what will be the count after 144 input pulses.

**PART - B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT - I**

- 2 Encode the decimal number 365 in  
(i) Binary (ii) BCD (iii) ASCII (iv) Excess - 3.  
OR
- 3 Given the 8 - bit data word 01011011 generate the 12 bit composite word for the hamming code that corrects and detects single errors.

**UNIT - II**

- 4 (a) Implement the Boolean expression for Ex-OR gate using NAND gates.  
(b) Simplify the Boolean expression  $\overline{AB}(\overline{D} + \overline{C}D) + B(A + \overline{A}CD)$  to one literal.  
OR
- 5 (a) Implement Ex- NOR gate using only NOR gates.  
(b) Use the K-map method to simplify the following 5-variable function  
 $F = \sum(3, 6, 7, 8, 10, 12, 14, 17, 19, 20, 21, 24, 25, 27, 31)$

**UNIT - III**

- 6 (a) What is a decoder? Construct  $3 \times 8$  decoder using logic gates and also write truth table.  
(b) Design a 4 bit odd parity generator. Mentions its truth table.  
OR
- 7 (a) Implement the following Boolean function using 8:1 multiplexer.  
 $F(A, B, C, D) = \overline{A}B\overline{D} + ACD + \overline{B}CD + \overline{A}\overline{C}D$   
(b) Design a 2 bit comparator using gates.

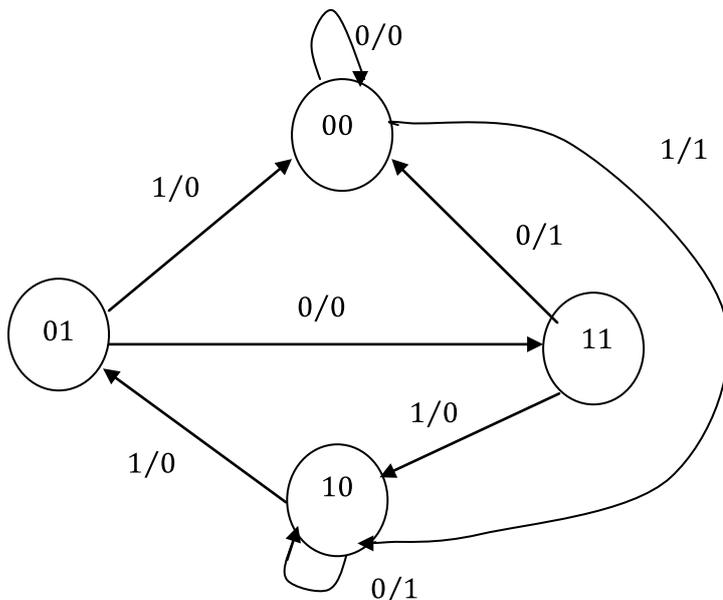
**UNIT - IV**

- 8 (a) Construct a JK flip-flop using D flip-flop,  $2 \times 1$  multiplexer and an inverter.  
(b) Convert SR flip - flop to T flip - flop.  
OR
- 9 Define the following terms in connection with a flip-flop  
(i) Setup time (ii) Hold time (iii) Propagation delay time (iv) Preset (v) Clear.

Contd. in page 2

UNIT - V

10 A sequential circuit has one input and one output. The state diagram is shown below:



Design the sequential circuit with (a) D flip-flop (b) RS flip-flop (c) JK flip-flop.

OR

11 (a) Implement the following Boolean function using PLA

$$F_1(w, x, y, z) = \sum(0,1,3,5,9,13)$$

$$F_2(w, x, y, z) = \sum(0,2,4,5,7,9,11,15)$$

(b) What is hazard in switching circuits? Explain the design of hazard free switching circuit with an example.

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B.Tech II Year I Semester (R13) Regular Examinations December 2014  
**SWITCHING THEORY & LOGIC DESIGN**  
 (Common to ECE and EIE)

Time: 3 hours

Max. Marks: 70

**PART – A**  
 (Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- If  $143_5 = X_6$ , then X is.....
  - Minimum number of two input NAND gates required to implement  $Y = A + B C$ .
  - What is the importance of don't care conditions?
  - SOP of  $F(x, y, z) = \sum(2, 3, 6, 7)$ .
  - Implement OR gate using only two input NAND gates?
  - Draw the block diagram of 2x4 decoder with enable.
  - Draw the block diagram of sequential circuit using combinational circuit and memory unit.
  - Draw the logic circuit of flip-flop and truth table using NOR gates.
  - What is the function of EAROM?
  - Mention few applications of PLA.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 (a) Convert the following to Decimal and then to Octal. (i)  $4234_{16}$  (ii)  $10010011_2$   
 (b) Implement the function with NOR-NOR logic  $Y = A C + B C + A B + D$ .
- OR
- 3 (a) Convert the following to Decimal and then to Hexadecimal. (i)  $1234_8$  (ii)  $11001111_2$   
 (b) Find the complement of the following Boolean function and reduce into minimum number of literals.  
 $Y = BC' + A'D)(DB' + CD'$

**UNIT – II**

- 4 Simplify the following Boolean expressions using K-map and implement them using NAND gates.  
 $F(W, X, Y, Z) = XZ + W'XY + WXY + W'YZ + W'YZ$
- OR
- 5 Simplifying the following expression using tabulation technique.  
 $F = \sum m(0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)$

**UNIT – III**

- 6 (a) Design a 4 bit binary-to-Gray code converter.  
 (b) Realize a 2-bit comparator.
- OR
- 7 (a) Design a 4 bit binary-to-BCD code converter.  
 (b) Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux.

**UNIT – IV**

- 8 (a) Draw the circuit of JK flip flop using NAND gates and explain its operation.  
 (b) Design a 2-input 2-output detector which produces an output 1 every time the sequence 0101 is detected. Implement the sequence detector using JK flip-flops.
- OR
- 9 (a) Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram.  
 (b) A clocked sequential circuit with single input x and single output z produces an output  $z=1$  whenever the input x compares the sequence 1011 and overlapping is allowed. Obtain the state diagram, state table and design the circuit with D flip-flops.

**UNIT – V**

- 10 (a) Explain about ROM and PROM.  
 (b) Design a BCD to excess-3 code converter using ROM.
- OR
- 11 (a) What is Race-free state Assignment? Explain.  
 (b) Realize  $f = \sum m(0, 2, 3, 7, 9, 11, 15, 16)$  using ROM.

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B.Tech II Year II Semester (R13) Supplementary Examinations May/June 2019

**SWITCHING THEORY & LOGIC DESIGN**

(Common to EEE and ECE)

Time: 3 hours

Max. Marks: 70

**PART – A**

(Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- Find the 10's complement of the decimal value  $012398_{10}$ .
  - Find the complement of the function  $F_1 = x(y'z' + yz)$  by applying DeMorgan's theorem as many times as necessary.
  - Simplify the Boolean function  $F(x, y, z) = \sum(0,1,5,7)$  using three-variable map.
  - Draw the logic diagram of a 3-bit even parity generator.
  - Given X-OR gate has a propagation delay of 20 ns and AND or OR gates have a propagation delay of 10 ns. Find the total propagation delay in a full adder.
  - Give the steps involved in designing a combinational circuit.
  - Define trigger in a flip-flop.
  - List out the applications of shift registers and counters.
  - An asynchronous sequential circuit is described by excitation function  $Y = x_1x_2' + (x_1 + x_2')y$ . Draw the logic diagram of the circuit.
  - Differentiate between RAM and ROM.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 (a) Simplify and draw the logic diagram for the given expression:

$$A = (ABC)' + (AB)'C + A'BC' + A(BC)' + AB'C$$

- (b) Simplify the following identities using Boolean algebra:

$$(A + B)(A + (AB)')C + A'(B + C') + A'B + ABC$$

**OR**

- 3 (a) State and prove DeMorgan's law of union.  
 (b) Express the Boolean function  $F = xy + x'z$  in a product of maxterm form.

**UNIT – II**

- 4 (a) Simplify the Boolean function  $F(w, x, y, z) = \sum(2,3,10,11,12,13,14,15)$  using four-variable K-map.  
 (b) Simplify the Boolean function  $(A' + B' + D')(A + B' + C')(A' + B + D')(B + C' + D')$  in sum of product.

**OR**

- 5 (a) Implement the Boolean function  $F = xy' + x'y' + z$  by using NAND gates.  
 (b) By using tabulation methods simplify the function:

$$Z = f(A, B, C) = A'B'C' + A'B'C + AB'C' + AB'C$$

**UNIT – III**

- 6 Derive the expression for BCD to excess-3 code converter using K-map and implement the combinational logic circuit of it.

**OR**

- 7 Implement the following functions using a multiplexer:

(i)  $F(x, y, z) = \sum(1,2,6,7)$

(ii)  $F(A, B, C, D) = \sum(1,3,4,11,12,13,14,15)$

Contd. in page 2

## UNIT – IV

- 8 Reduce the number of states in the following state table and tabulate the reduced state table shown below:

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

OR

- 9 With a neat circuit diagram and function table, explain the logical operation of a 4-bit universal shift register in detail.

## UNIT – V

- 10 Explain in detail about the design procedures involved with designing an asynchronous sequential circuit by minimizing the circuit complexity and producing a stable circuit without critical races.

OR

- 11 (a) Draw the timing waveforms for read and write memory cycle in a Random Access Memory.  
 (b) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number.

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**SWITCHING THEORY & LOGIC DESIGN**

(Common to EEE and ECE)

Time: 3 hours

Max. Marks: 70

**PART – A**

(Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- State and Prove consensus theorem.
  - Find the 2's complement of representation of -9.
  - Design a XOR gate using minimum number of NAND gates.
  - Find the minimum number of literals for the following function using 2 variable Karnaugh Map.  
 $F = \sum m(1) + d(3)$ . d - Don't care.
  - Write the sum and carry expression for half adder.
  - Implement the function  $F = \sum m(0, 2)$  using a  $2 \times 4$  decoder.
  - Write the characteristic equation for JK Flip-flop.
  - How many states are there in a n-bit ring counter?
  - Compare PROM & PAL.
  - What is meant by cycle in asynchronous circuits?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 (a) Express the following function  $F = xy + x'y$  in a product of max-terms.  
 (b) Check if NOR gate is associative or not.

**OR**

- 3 (a) Show that a positive logic NAND gate is a negative logic OR gate  
 (b) Obtain the truth table of the following function and express in sum of min-terms and product of max-terms:  $F = (A' + B).(B' + C)$ .

**UNIT – II**

- 4 Simplify the Boolean function using K map technique:  
 (a)  $F = \pi M(3, 4, 6, 7, 11, 12, 13, 14, 15)$ .  
 (b)  $F = \sum m(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$ .

**OR**

- 5 Simplify the following Boolean function using tabulation method:  
 $F = \sum m(0, 1, 2, 3, 5, 7, 8, 10, 14, 15)$ .

**UNIT – III**

- 6 Design a 4-Bit Magnitude comparator using logic gates.

**OR**

- 7 (a) Implement the function  $F = \sum m(0, 1, 2, 4, 5, 8, 11, 12, 15)$  using 8:1 multiplexer.  
 (b) Design a half subtractor using logic gates.

**UNIT – IV**

- 8 Design a 4 bit universal shift register with neat diagram.

**OR**

- 9 Design a 3 bit synchronous up counter using T Flip-flops.

**UNIT – V**

- 10 Implement the following functions using PLA with three inputs, four product terms and two outputs.  
 $F_1(A, B, C) = \sum m(3, 5, 6, 7)$ ,  $F_2(A, B, C) = \sum m(0, 2, 4, 7)$ .

**OR**

- 11 Implement the switching function  $F = \sum m(1, 3, 5, 7, 8, 9, 14, 15)$  by a static hazard free two level AND-OR network.

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B.Tech II Year I Semester (R13) Supplementary Examinations November/December 2018

**SWITCHING THEORY & LOGIC DESIGN**

(Common to ECE &amp; EIE)

Time: 3 hours

Max. Marks: 70

**PART – A**

(Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- Draw the symbol of universal gates.
  - State the Demorgan's theorem.
  - Expand POS and SOP.
  - Realize AND operation by using NAND gates.
  - Define decoder.
  - Mention two applications multiplexer.
  - What is the drawback of SR latch?
  - Define counter.
  - List out the types of PLDs.
  - Define hazards in logic design.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 (a) Perform subtraction by using 10's complement for the given 845-245.  
 (b) Perform subtraction by using 2's complement for the given 111011-1010.

**OR**

- 3 Interpret the following to decimal and then to binary:  
 (i)  $10111_6$ . (ii)  $ABCD_{16}$ . (iii)  $7234_8$ . (iv)  $1100_2$ .

**UNIT – II**

- 4 Minimize using K-map and realize by NAND gates  $F(A,B,C,D) = \Sigma(0,1,2,3,12,13,14,15)$ .

**OR**

- 5 (a) Minimize and realize,  $F = \overline{(\overline{X} + \overline{Y} + Z)} + Z + WZ$  by basic gates.  
 (b) Realize Ex-OR and Ex-NOR gate operations by NOR gates.

**UNIT – III**

- 6 Construct BCD adder and explain the operation.

**OR**

- 7 (a) Implement  $F = \Sigma(0,1,2,3)$  using decoder,  
 (b) Design 3X3 binary multiplier.

**UNIT – IV**

- 8 (a) Develop 3 bit ripple up counter.  
 (b) Create the circuit of JK flip-flop using NAND gates and explain its operation.

**OR**

- 9 (a) Derive the characteristics table and characteristic equation of DFF.  
 (b) Design T flip flop by using SR flip flop.

**UNIT – V**

- 10 (a) Write the differences between PAL and PLA.  
 (b) Minimize and implement the Boolean function  $F = \Sigma(0,1,2,3,13,14,15)$  using PROM.

**OR**

- 11 Explain about analysis procedure in sequential circuits in detail.

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B.Tech II Year I Semester (R15) Supplementary Examinations June 2018  
**SWITCHING THEORY & LOGIC DESIGN**  
 (Common to ECE & EIE)

Time: 3 hours

Max. Marks: 70

**PART – A**  
 (Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- (a) Converting the following to decimal and then to octal:  
 (i)  $(4243)_{16}$ . (ii)  $(125F)_{16}$ .
  - (b) Write are the steps for tabular method-simplification of Boolean function?
  - (c) Design procedure for combinational logic circuits.
  - (d) Write the differences between Latches and Flip-Flops.
  - (e) Give design procedure for asynchronous sequential circuits.
  - (f) Define EPROM and EEPROM.
  - (g) Write the basic definition for Boolean algebra.
  - (h) Give comparison between POS and SOP.
  - (i) What is multiplexer with example?
  - (j) Briefly explain about D-flip-flop.

**PART – B**  
 (Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 (a) Explain Logic Operations and logic gates with examples.  
 (b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend: (i)  $11010-10000$ . (ii)  $11010-1101$ . (iii)  $1010100-1010100$ .

OR

- 3 (a) Why the binary number system is used in computer design? And what is the necessity of binary codes?  
 (b) Perform the following using BCD arithmetic. Verify the result:  
 (i)  $1273_{10} + 9587_{10}$ . (ii)  $7762_{10} + 3838_{10}$ . (iii)  $7842_{10} + 4956_{10}$ .

**UNIT – II**

- 4 Implement the function F with the following two level forms:  
 (i) NAND-AND. (ii) AND-NOR. (iii) OR-NAND. (iv) NOR-OR.  
 $F(A,B,C,D) = \pi (0,1,2,3,4,8,9,12)$

OR

- 5 Minimize following function using Tabular minimization:  
 $F(A,B,C,D) = \pi M (6,7,8,9) + d(10,11,12,13,14,15)$

**UNIT – III**

- 6 (a) What is decoder? Construct  $3 \times 8$  decoder Using logic gates and truth table.  
 (b) Implement the following multiple output combinational logic using 4 line to 16 line decoder?
- OR
- 7 (a) Design a combinational logic to subtract one bit from the other. Draw the logic diagram using NAND and NOR gates.  
 (b) Explain the function of Digital magnitude comparator using a neat diagram.

Contd. in page 2

**UNIT – IV**

- 8 (a) Convert the following: (i) JK flip-flop to T flip-flop. (ii) RS flip-flop to D flip-flop.  
(b) Draw the circuit diagram of 4-bit Ring Counter D flip-flop and explain its Operation with the help of bit pattern.

**OR**

- 9 (a) Compare synchronous and asynchronous Sequential circuits with examples.  
(b) Design a Mod-6 synchronous counter using JK flip-flops? With state Table and K-map simplification.

**UNIT – V**

- 10 (a) Derive the PLA programming table for the combinational circuit that squares a 3-bit number.  
(b) Design a BCD to excess-3 code convert using: (i) ROM. (ii) PAL.

**OR**

- 11 (a) A combinational circuit is defined by the functions:

$$F_1 = (A,B,C) = \pi m(3,5,6,7)$$

$$F_2 = (A,B,C) = \pi m(0,2,4,7)$$

Implement the circuit with a PAL having three inputs, four product terms and two outputs.

- (b) Explain the field programmable gate array (FPGA) with suitable block diagram.

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**DIGITAL ELECTRONICS & LOGIC DESIGN**

(Common to EEE & ECE)

Time: 3 hours

Max. Marks: 70

**PART – A**

(Compulsory Question)

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- 1 Answer the following: (10 X 02 = 20 Marks)
- Convert the binary number {1101010101111011} into hexadecimal number.
  - Draw the symbol and truth table of XOR gate.
  - Draw the logical diagram of half subtractor.
  - Draw the schematic diagram of 1:2 decoders.
  - Write short notes on state table.
  - Write short notes on counters.
  - Compare RAM and ROM.
  - List the classification of ROM.
  - Compare TTL with RTL.
  - Write short notes on FAN out.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 Simplify the Boolean function using K-map techniques:  
 $F(w, x, y, z) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$ .  
 $F = AB + (ABC)' + (B'C' + C) + (AC)'$

OR

- 3 Explain the operation of XOR, NAND, NOR operation using logic gates, truth tables, and timing diagram.

**UNIT – II**

- 4 Draw and explain the logic circuit diagram and truth table of 8:1 multiplexer.

OR

- 5 Explain RS, D and T flip flops with block diagram and truth table.

**UNIT – III**

- 6 Construct the mealy circuit to detect the sequential inputs of 10110. Assume the suitable parameters.

OR

- 7 Explain the operation of synchronous up/down counter using suitable circuit.

**UNIT – IV**

- 8 Explain the logic circuit diagram of PLA.

OR

- 9 Implement BCD to excess-3 code converter using PLD.

**UNIT – V**

- 10 Explain the circuit diagram of TTL with active pull up and open collector output.

OR

- 11 Explain the construction and characteristics of CMOS inverter.

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