Presentation
Of
RF INTEGRATED CIRCUITS
(UNIT-IV : POWER AMPLIFIERS)

BY

M.JYOTHIRMAI
ASSISTANT PROFESSOR
Department of ECE

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN
Kurnool-518452,Andhra Pradesh,INDIA

CONTENTS

Power Amplifier Characteristics

- Function: Deliver power to antenna
- Power Dissipation easily dominates the transceiver power budget
- Key Specification:
  - Maximum Output Power
  - Efficiency/Power Added Efficiency
  - Power Gain
  - Linearity
  - Stability
  - Radiation Pattern
  - Thermal Emission

PERFORMANCE METRICS

- Output Power
- Efficiency
- Linearity

Output Power

- **Power delivered to the load within the band of interest.**
- **Load is usually an antenna with Z0 of 50Ω**
- **Doesn't include power contributed by the harmonics or any unwanted spurs**

- **Sinusoidal**

$$P_{out} = \frac{V_{out}^2}{2R_L}$$

- **Modulated Signal**

$$P_{out/avg} = \int_0^{\infty} \varphi(p)\,dp = \frac{1}{T}\int_0^{T} v(t)\,dt$$

Probability profile of Modulation: *Prob* (P_{out}=p)

Efficiency

- *Power Added Efficiency* → **Most common efficiency metric**
- **DC→ RF**

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \times 100\%$$

- **Shows how efficiently supply DC power is converted to RF power**
- **Drain efficiency is often used to indicate the efficiency of a single power amplifier stage**

$$\eta_{drain} = \frac{P_{delivered}}{P_{DC}} \times 100\%$$

Linearity

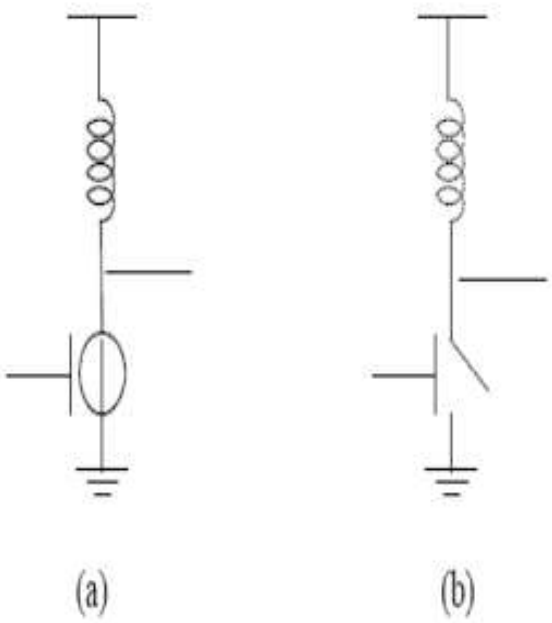
- **Linearity Requirement can be different based on modulation**
  - **Variable Envelope**
    - **Information is carried in the amplitude**
    - **$\prod/4$ *DQPSK* and *OQPSK***
  - **Constant Envelope**
    - **Information is carried in the phase**
    - ***GMSK* and *GFSK***

CLASSIFICATION OF RF POWER AMPLIFIER

- Linear
- Switch mode

- **Linear PA: Class A,B,AB and C**
  - **transistor acts as a current source**
  - **Since certain amount of voltage must exist to keep the device in the current source mode, there is always certain power dissipation on the device**
- **Switch mode PA: Class D,E,F**
  - **Active device acts as a switch**
  - **There is either zero voltage across or zero current through a switch**

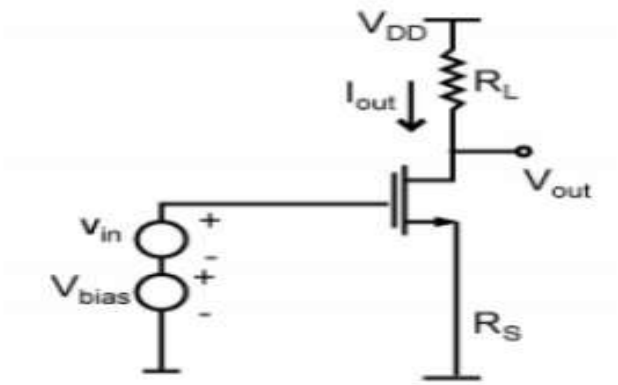
➔ **100% efficiency possible**

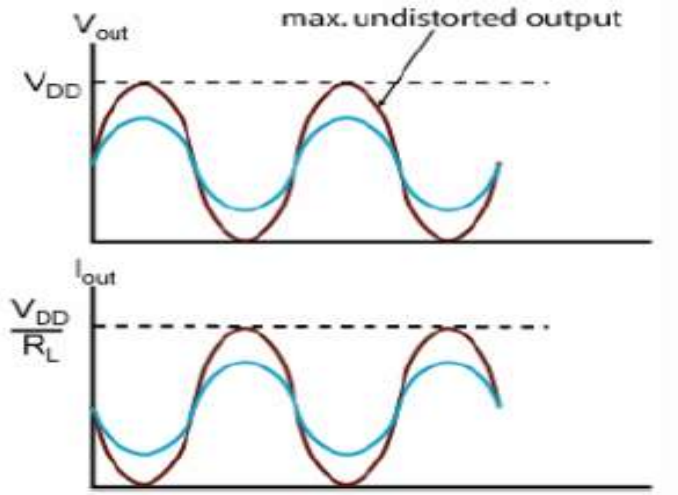


1.CLASS A POWER AMPLIFIER

Resistor Loaded Class A Amplifier

- In a Class A amplifier, the active device conducts current 100% of time
- For maximum output swing (and thus output power), the quiescent output voltage is set at $V_{DD}/2$, and bias current at $V_{DD}/2R_L$





Other Power Efficiency Parameters

- **Normalized Power Output Capability P_N**
  - **Ratio between power delivered to load and peak current times peak voltage on the output device**
  - **Measure related to output device power handling**

$$P_N = \frac{P_{L,max}}{v_{DS,max} \cdot i_{D,max}} = \frac{\frac{V_{DD}^2}{8R_L}}{V_{DD} \cdot \frac{V_{DD}}{R_L}} = \frac{1}{8}$$

- **Power Added Efficiency (PAE)**
  - **Added signal power by the amplifier divided by DC biasing power**

$$PAE = \frac{P_L - P_{in}}{P_{DC}}$$

  - **At low frequencies, PAE=η for the previous amplifier**

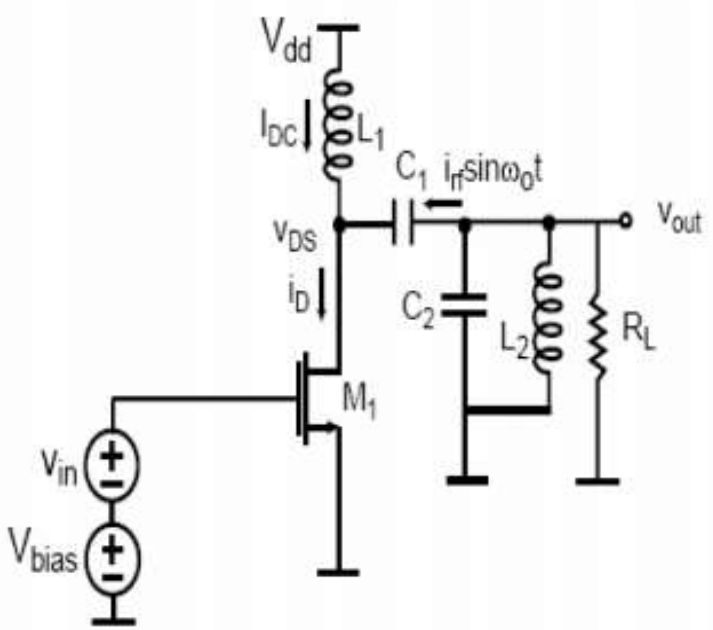
Class A RF Power Amplifier

- **Inductor improves peak amplitude, thus power efficiency**

L1: Large inductor: acts as current source

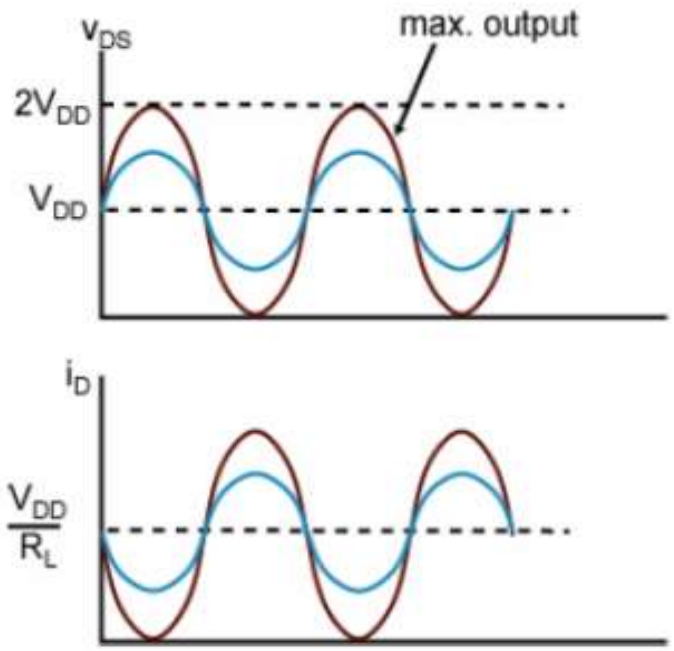
C1: DC block (prevents DC power in RL)

L2, C2: Output tank circuit



Drain Voltage and Current Waveforms

- **Since L1 presents a DC short to VDD, the drain voltage waveform must be symmetric around VDD. the maximum amplitude of sinusoid at the drain is VDD.**
- **The drain voltage (and the output voltage) swings to twice the power supply! (in practice limited by device breakdown)**



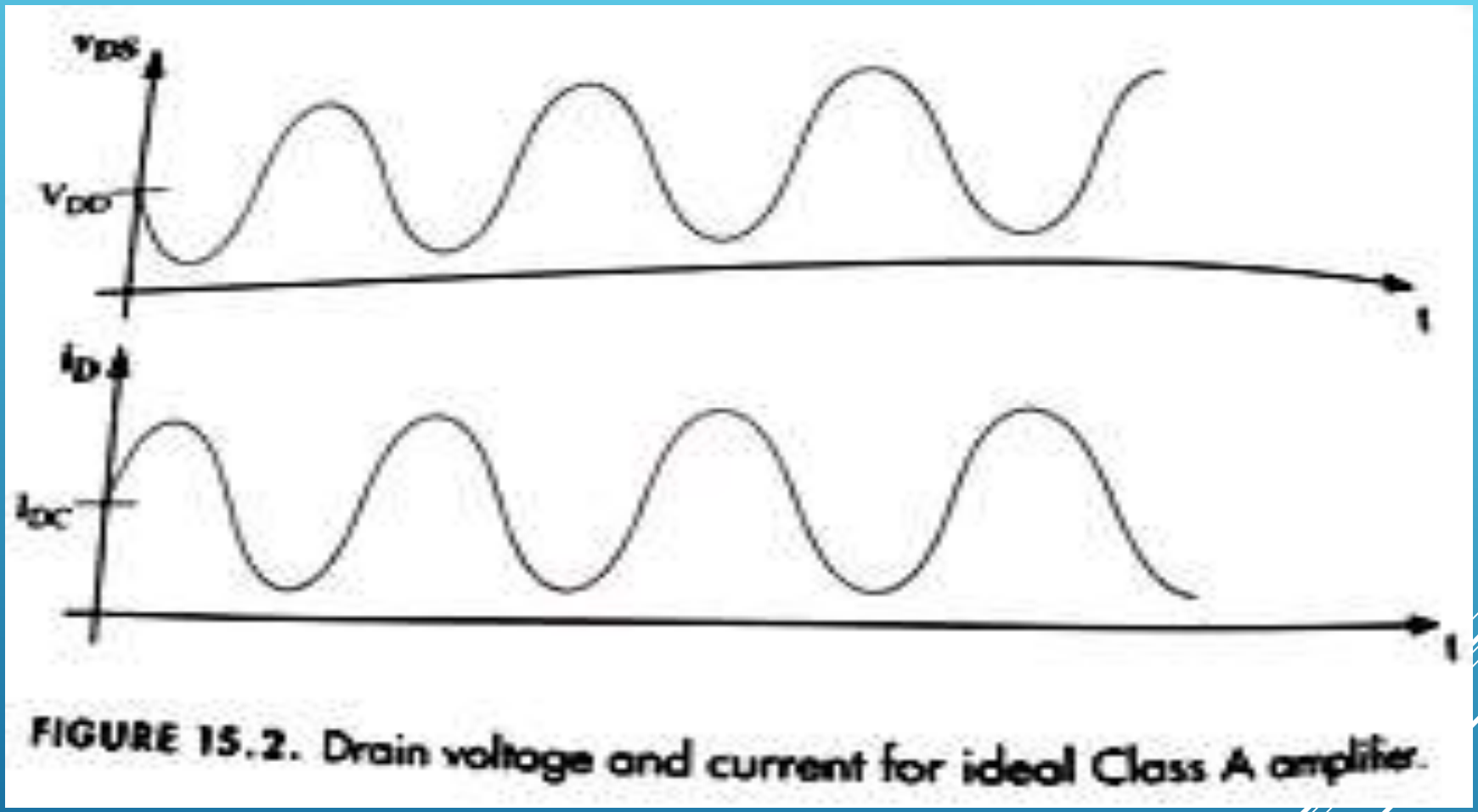


FIGURE 15.2. Drain voltage and current for ideal Class A amplifier.

Normalized Power Output Capability

$$P_N = \frac{P_{L,max}}{v_{DS,max} \cdot i_{D,max}}$$

$$P_{L,max} = \frac{V_{DD}^2}{2R_L}$$

$$v_{DS,max} = 2V_{DD} \qquad i_{D,max} = \frac{2V_{DD}}{R_L}$$

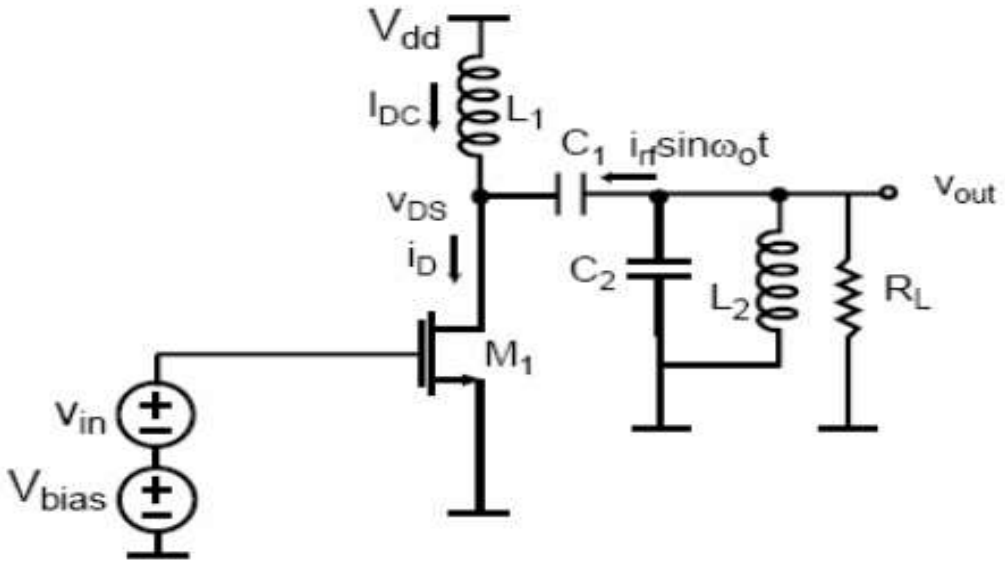
$$P_{N,max} = \frac{1}{8}$$

Class A amplifiers are linear, but have poor efficiency!

2.CLASS B POWER AMPLIFIER

Class B Power Amplifier

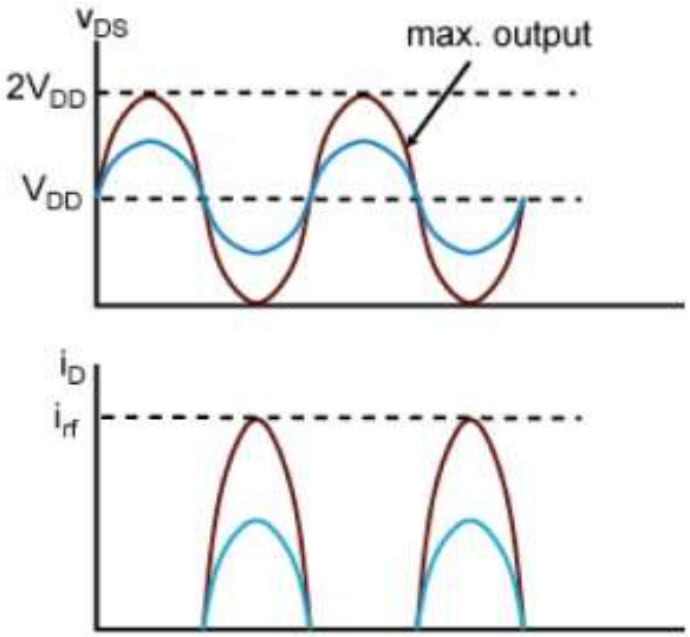
- Same circuit, but V_{bias} is set so that M1 conducts only 50% of time



$$V_{bias} \approx V_T$$

Class B Power Amplifier

- V_{bias} is set so that M1 conducts only 50% of time
- The harmonics in the output waveform are filtered by output tank circuit
- The fundamental component is a linear function of the input



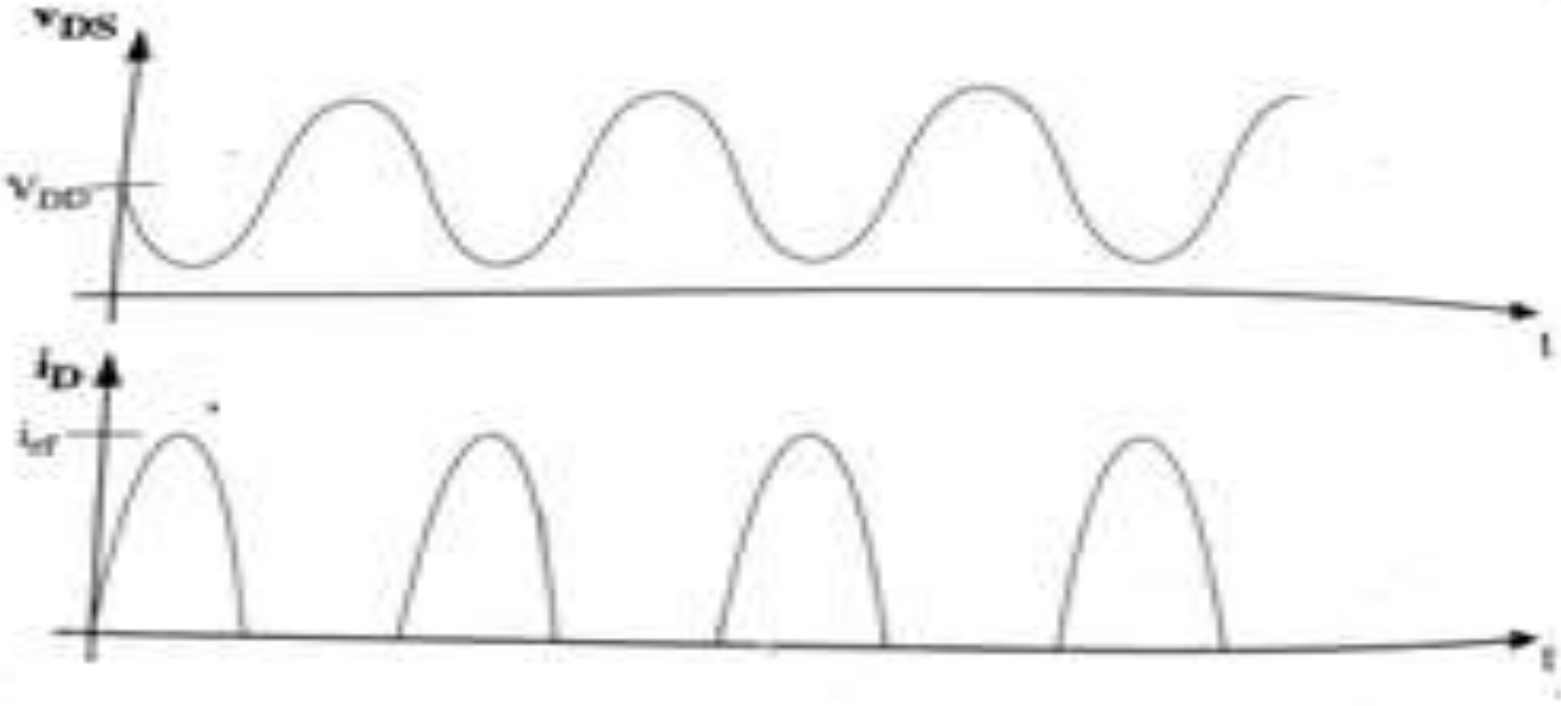


FIGURE 15.3. Drain voltage and current for ideal Class B amplifier

Class B Power Efficiency, Continued

- The DC component of max. i_D half-sine wave is

$$\overline{i_D} = \frac{1}{T}\int_0^{T/2} \frac{2V_{DD}}{R_L} sinw_o t dt = \frac{2V_{DD}}{\pi R_L}$$

- The DC power is then $P_{DC} = \frac{2V_{DD}^2}{\pi R_L}$
- And the efficiency $\eta = \frac{\pi}{4} = 0.785$
- Normalized Output Power Capability:

$$v_{DS,max} = 2V_{DD} \qquad i_{D,max} = i_{rf} \leq \frac{2V_{DD}}{R_L}$$

$$P_{L,max} = \frac{V_{DD}^2}{2R_L} \qquad P_N = \frac{P_L}{v_{DS,max} \cdot i_{D,max}} = \frac{1}{8}$$

Same as Class A

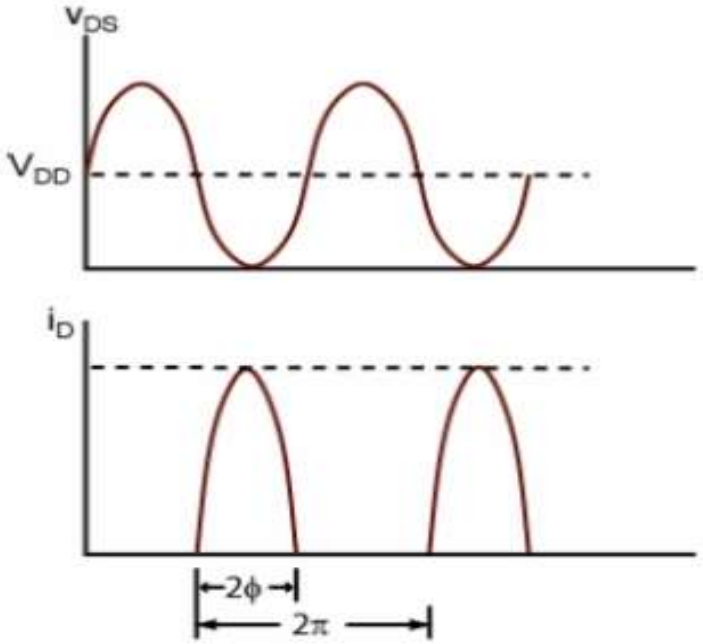
- Since DC power is proportional to the amplitude, η is proportional to square root of output power: slower degradation at lower power than class A

Conduction Angle vs. Class

- Conduction Angle φ :2φ is the portion of period during which the output transistor M1 conducts

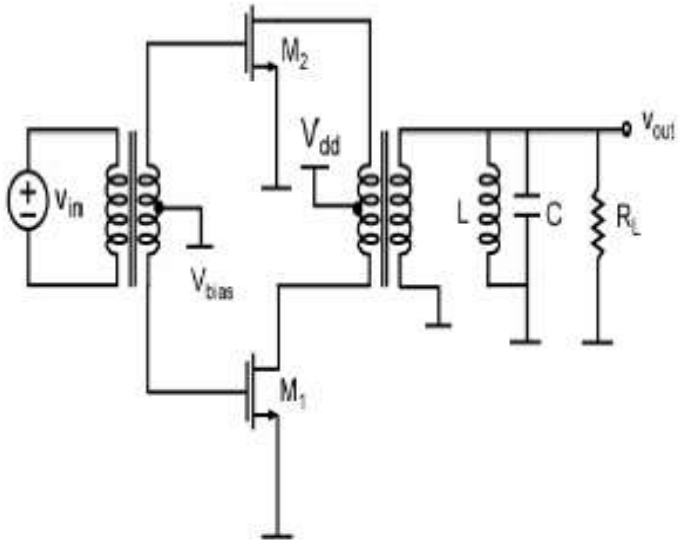
$2\varphi=2\pi$: Class A
$\pi<2\varphi<2\pi$: Class AB
$2\varphi=\pi$: Class B
$0<2\varphi<\pi$: Class C

(Class AB or C output cannot be a linear function of input)

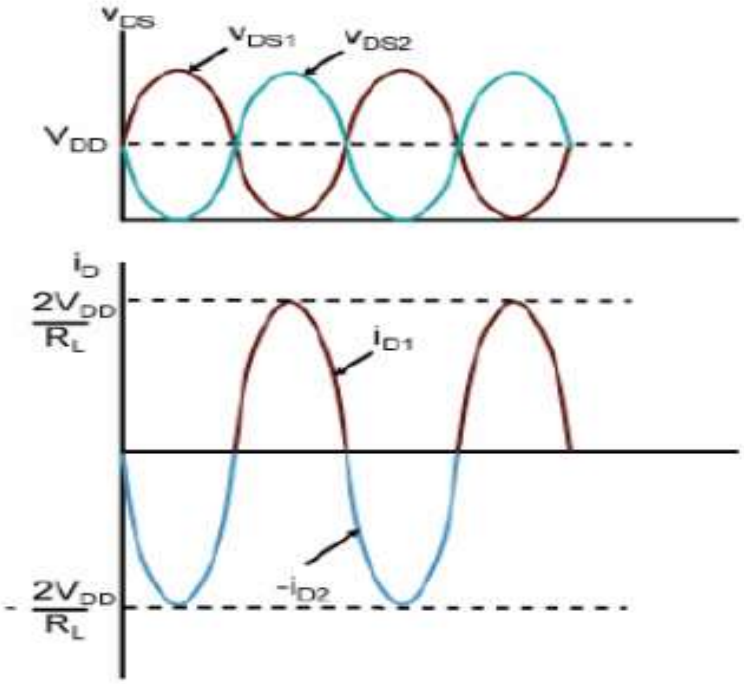


Push-Pull Amplifier

- Depending on V_{bias} and V_{in} push pull amplifier can be operated as Class A, B, AB, C, or D amplifier.
- Theoretically a Class B push pull amplifier has low distortion comparable to class A because either half will be conducting at any time.
- Real Class B is not possible because devices do not have abrupt turn- on characteristic–most are Class AB



Voltage and Current Waveforms of Class B Push-Pull

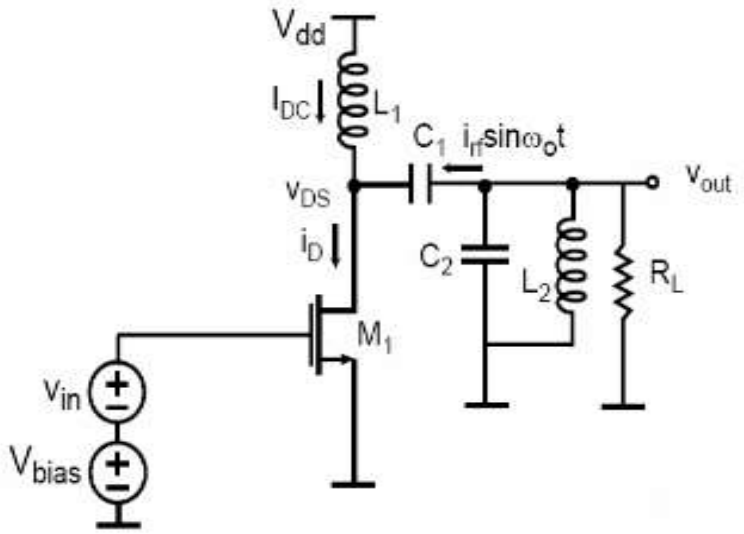


- Waveforms shown for maximum amplitude output
- typically, 'crossover distortion' arises at the switching point of the two halves due to imprecise turn-on voltages
- Crossover distortion is reduced by class AB operation

3.CLASS C POWER AMPLIFIER

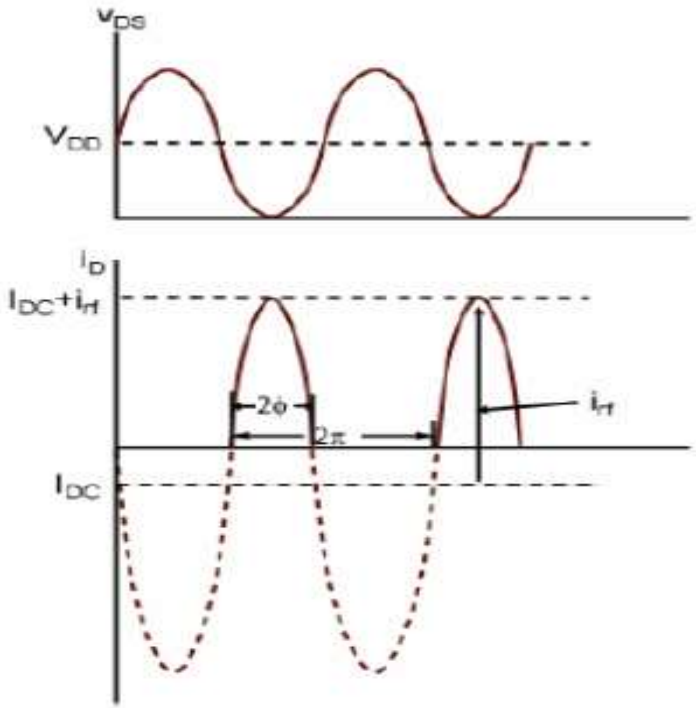
Class C Amplifier

- Same amplifier, but biased to conduct less than 50% of time
- The output amplitude is not a linear function of input: more suitable for constant-amplitude power amp (such as in PM or FM)



$$V_{bias} < V_T$$

Class C Amplifier Waveforms



$$i_D = I_{DC} + i_{rf} sinw_o t$$

$$i_D > 0, I_{DC} < 0$$

Conduction angle

$$2\phi = 2 \cdot cos^{-1}\left(-\frac{I_{DC}}{i_{rf}}\right)$$

Solving for the DC bias to achieve conduction angle φ

$$I_{DC} = -i_{rf} cos\phi$$

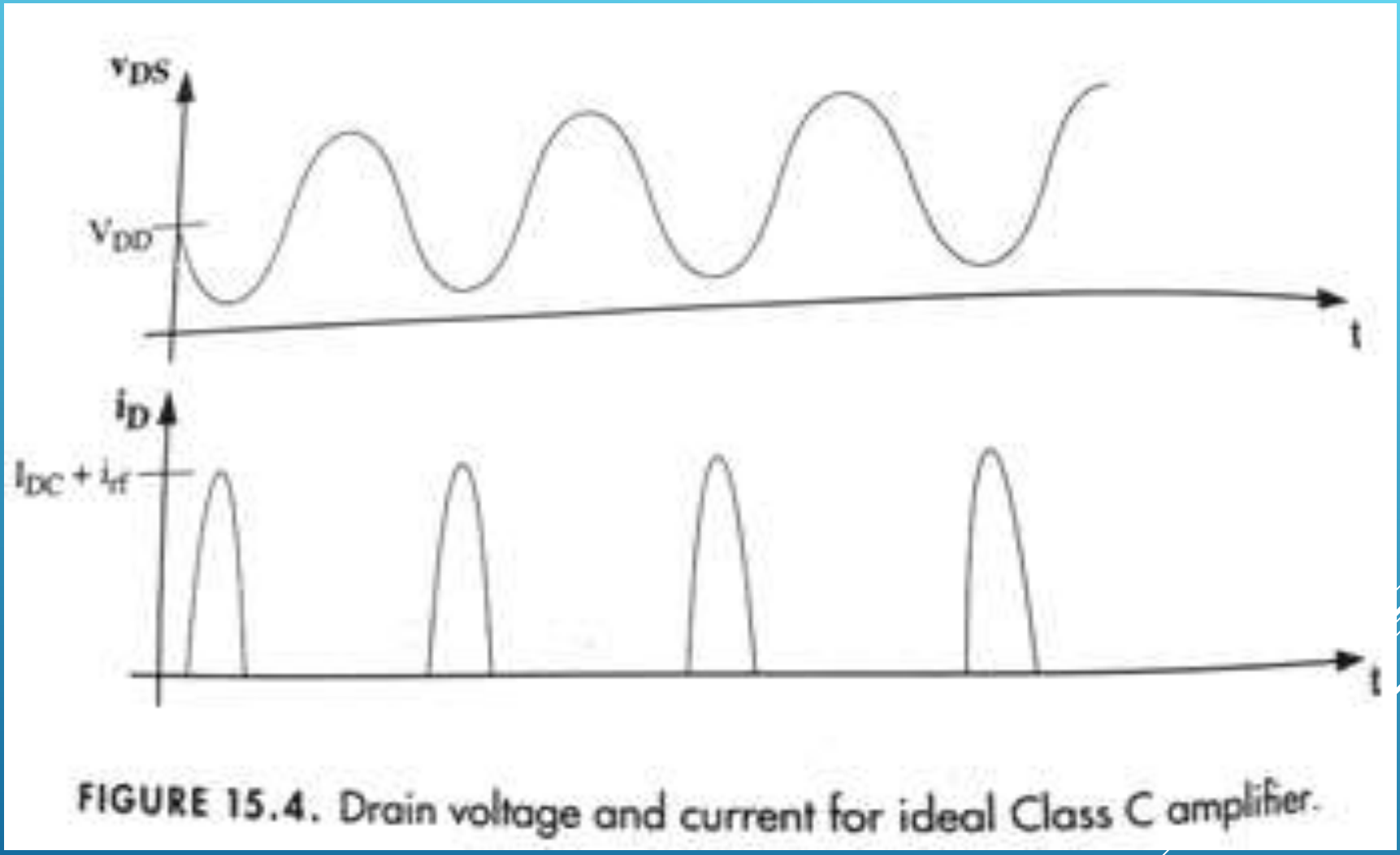


FIGURE 15.4. Drain voltage and current for ideal Class C amplifier.

Class C Power Efficiency Calculation

- **The average value of i_D**

$$\overline{i_D} = \frac{1}{2\pi}\int_{-\phi}^{\phi}\left(I_{DC} + i_{rf}cos\phi\right)d\phi = \frac{1}{2\pi}2\phi I_{DC} + \frac{1}{2\pi}\left[i_{rf}sin\phi\right]_{-\phi}^{\phi}$$

$$I_{DC} = \frac{i_{rf}}{\pi}\left(sin\phi - \phi cos\phi\right)$$

- **The fundamental component of i_D**

$$i_{fund} = \frac{2}{T}\int_0^T i_D cos w_o t dt = \frac{1}{2\pi}(4I_{DC}sin\phi + 2i_{rf}\phi + i_{rf}sin2\phi)$$

$$= \frac{i_{rf}}{2\pi}\left(2\phi - sin2\phi\right)$$

- **Maximum output swing is reached when**

$$i_{fund}R_L = V_{DD}$$

Class C Power Efficiency, Continued

- **Maximum efficiency is then**

$$\eta = \frac{2\phi - sin2\phi}{4\,(sin\phi - \phi cos\phi)} \qquad \phi \to 0 : \eta \to 1$$

- **The normalized output capability is poor at small conduction angles**

$$v_{DS,max} = 2V_{DD}$$

$$\phi \to 0 : i_{D,max} \to \infty, P_N \to 0$$

- **Thus, the efficiency must be sacrificed for reasonable P_N**

4.CLASS D POWER AMPLIFIER

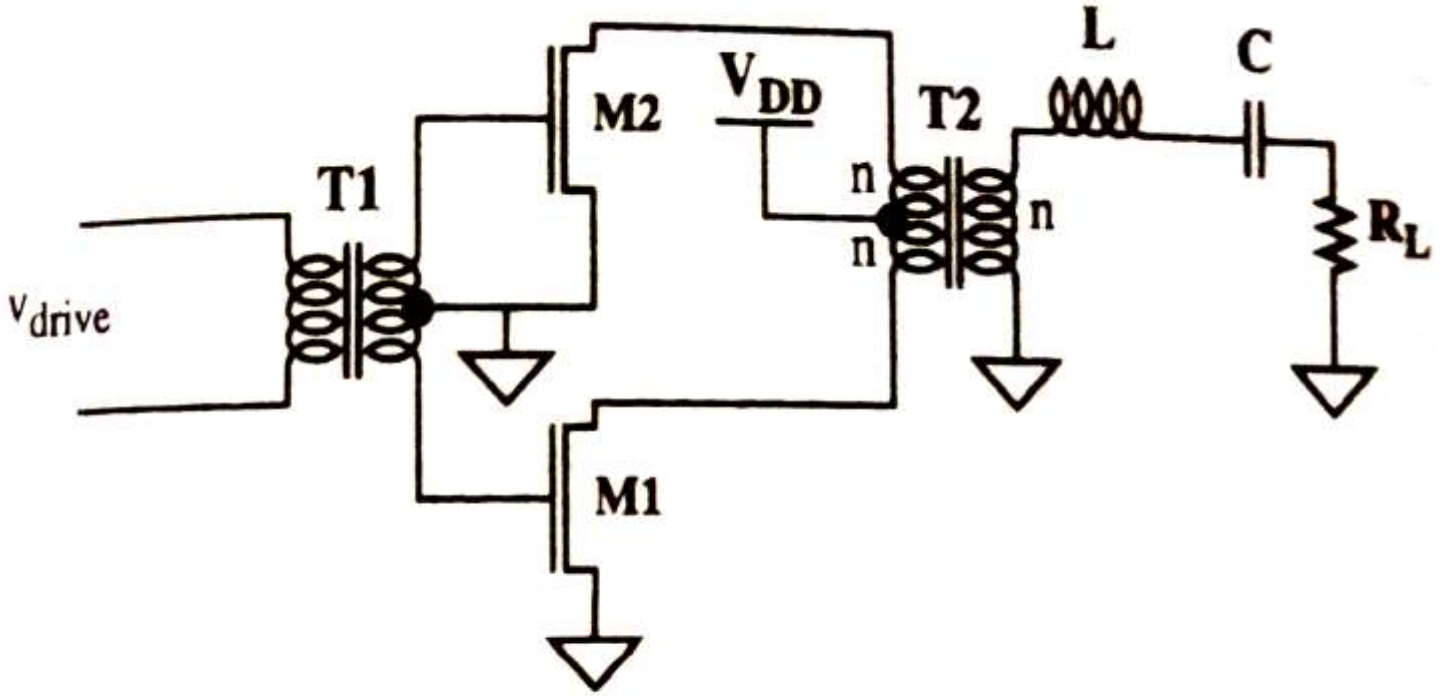


FIGURE 15.6. Class D amplifier.

Class D Amplifier Power Efficiency

- With ideal switches, Class D amplifier efficiency would be 100%
- In practice, finite switch ON resistance and nonzero on-off transients limit efficiency (use high f_t device!)
- In biploar Class D amplifier, the efficiency is further comprised due to charge storage in saturation and $V_{CE,SAT}$.
- Normalized power capability is shown to be

$$P_N = \frac{P_L}{v_{DS,max} \cdot i_{D,max}} = \frac{1}{\pi} = 0.32$$

5.CLASS E POWER AMPLIFIER

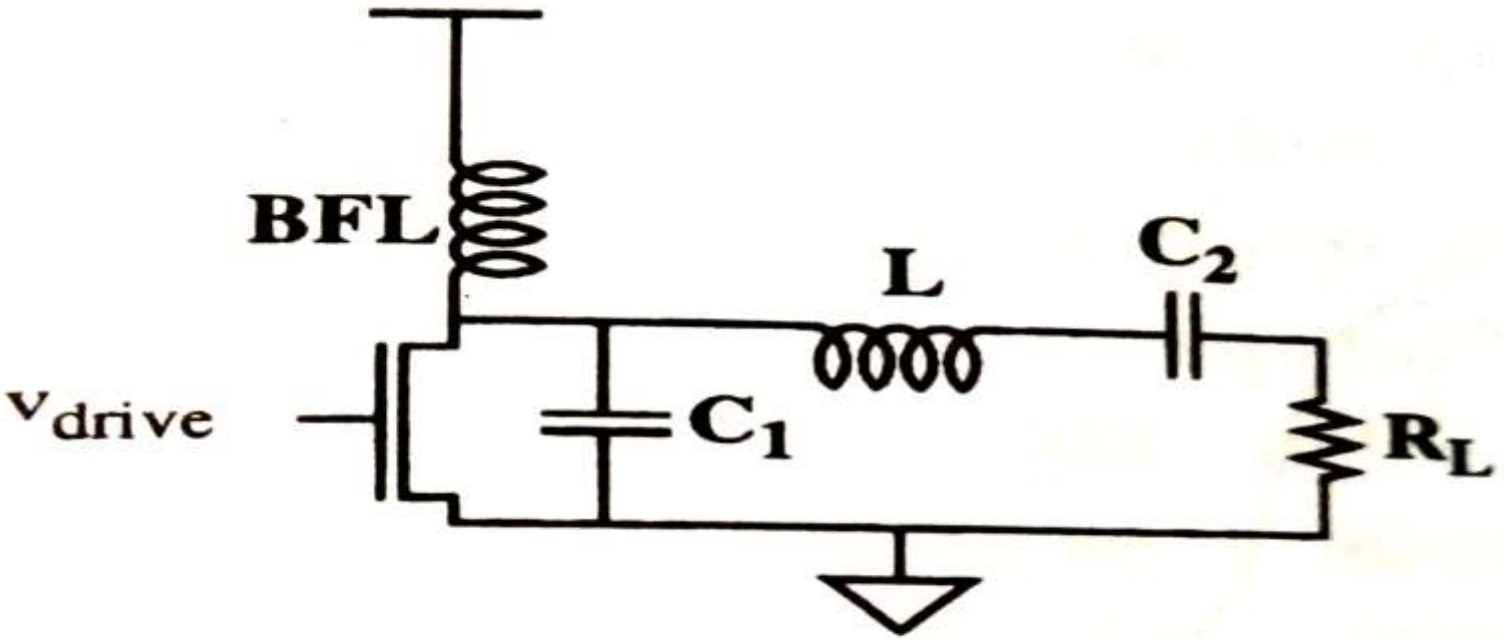
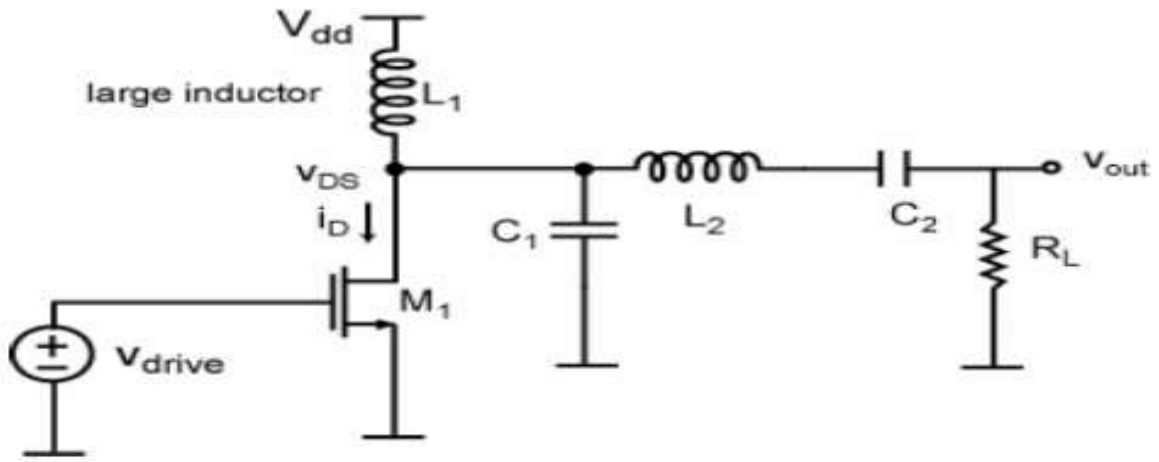


FIGURE 15.9. Class E amplifier.

Class E Power Amplifier

- Finite switching speed causes v-i product at the switching instant non-zero -> power loss
- Class E amplifiers tries to make both v and I zero at the off-to-on transients (solves only half of the problem)



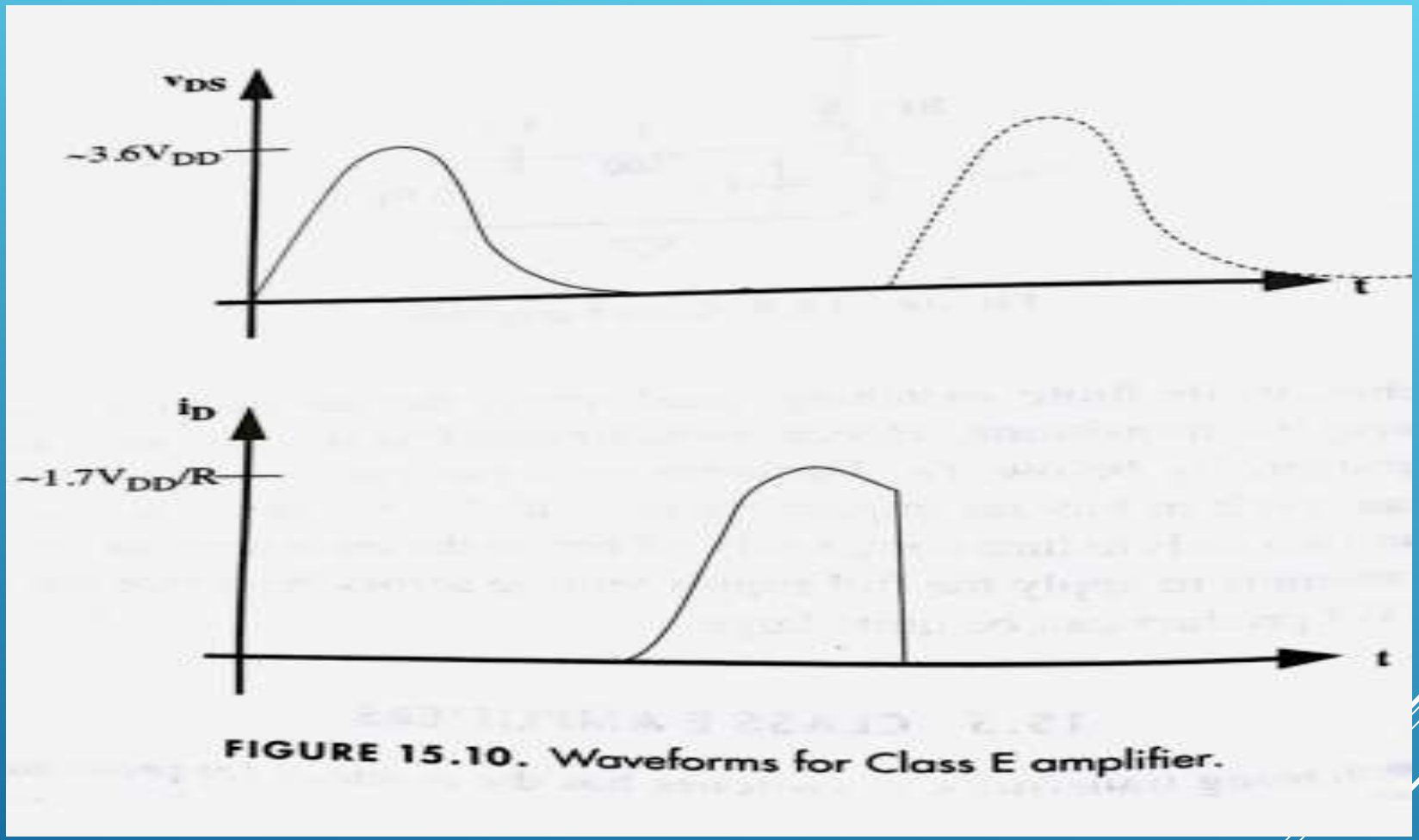
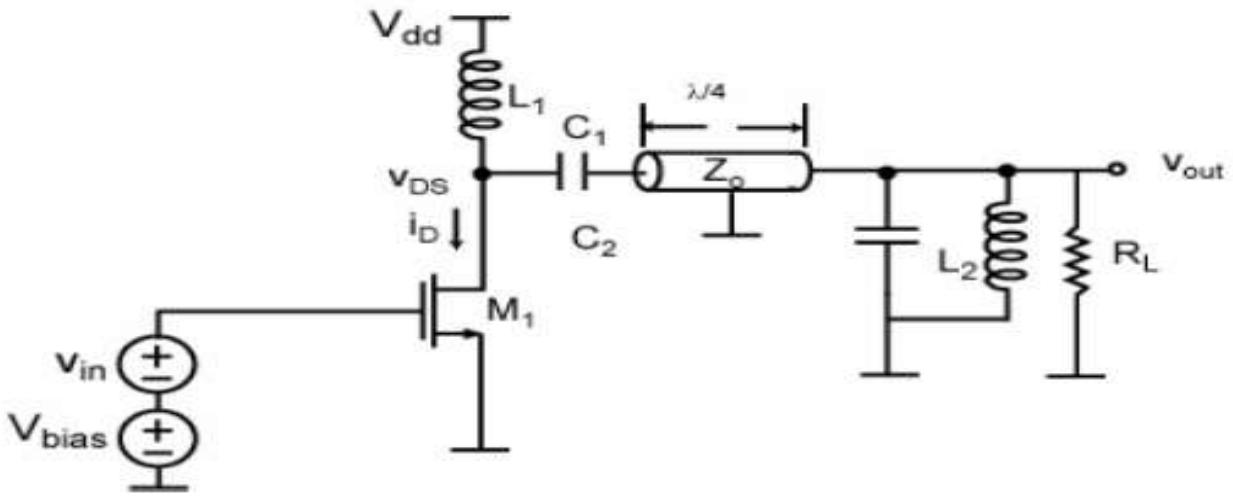


FIGURE 15.10. Waveforms for Class E amplifier.

6.CLASS F POWER AMPLIFIER

Class F Power Amplifier

- Allows square wave on drain
- Single-ended version of class D



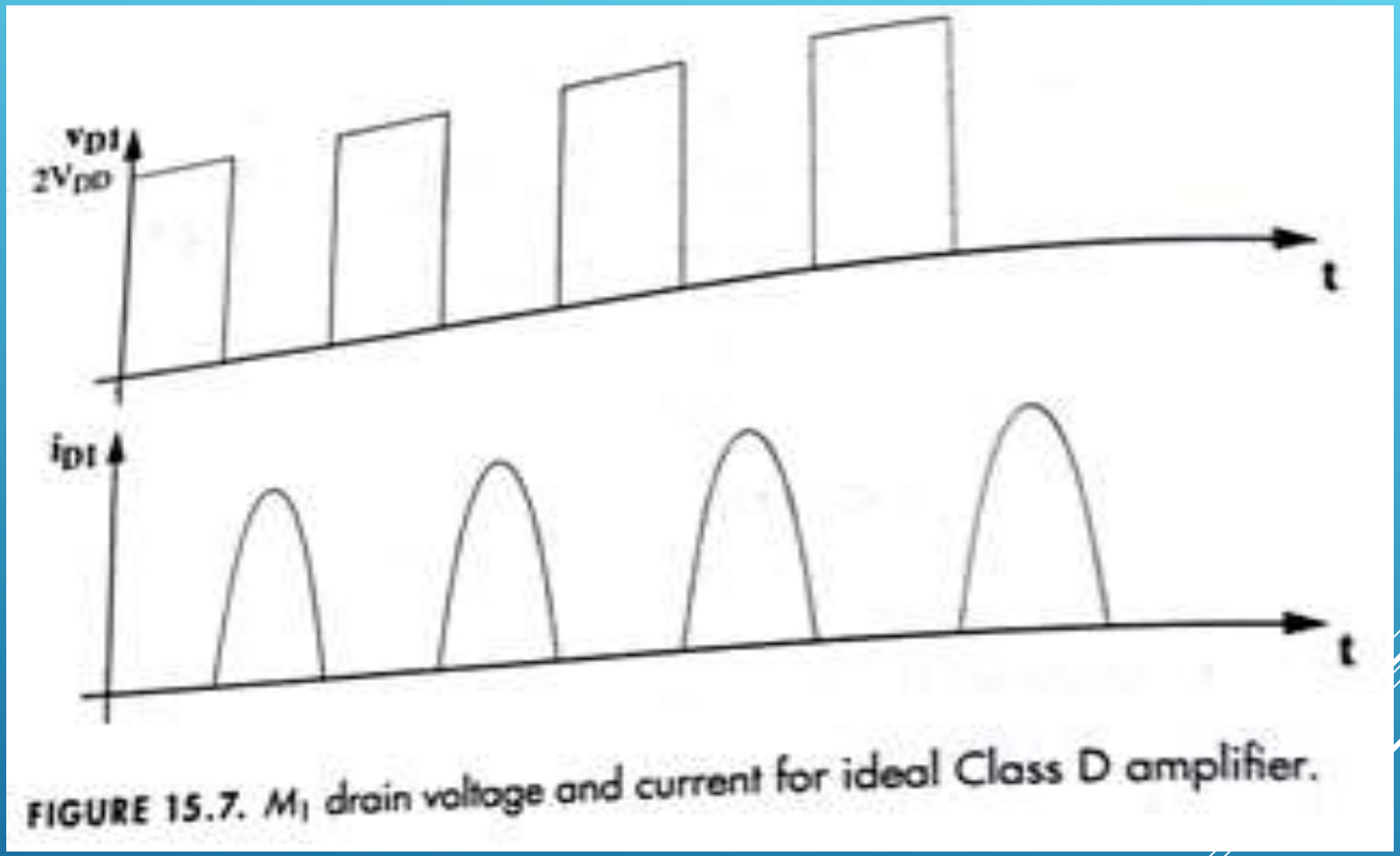
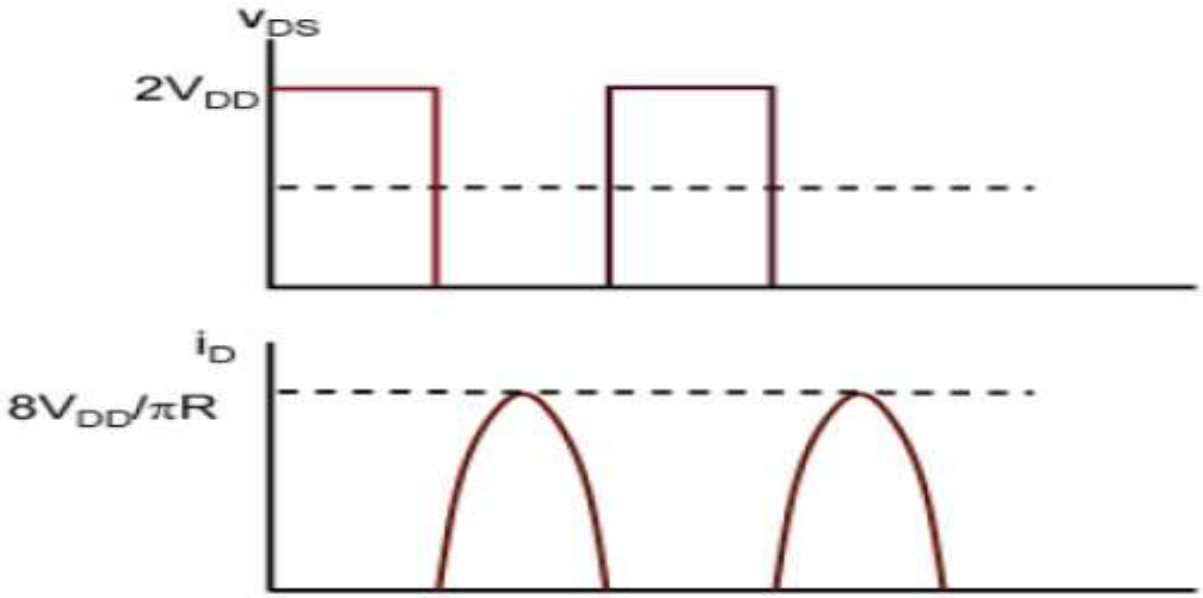


FIGURE 15.7. M_1 drain voltage and current for ideal Class D amplifier.

Class F Power Amplifier Waveforms

- The waveforms are similar to half of class D Push-Pull



Class F Power Amplifier Analysis

- **Refer Thomas. H. Lee's book**

Amplitude of fundamental frequency of drain voltage

$$v_{fund} = \frac{4}{\pi} \cdot V_{DD}$$

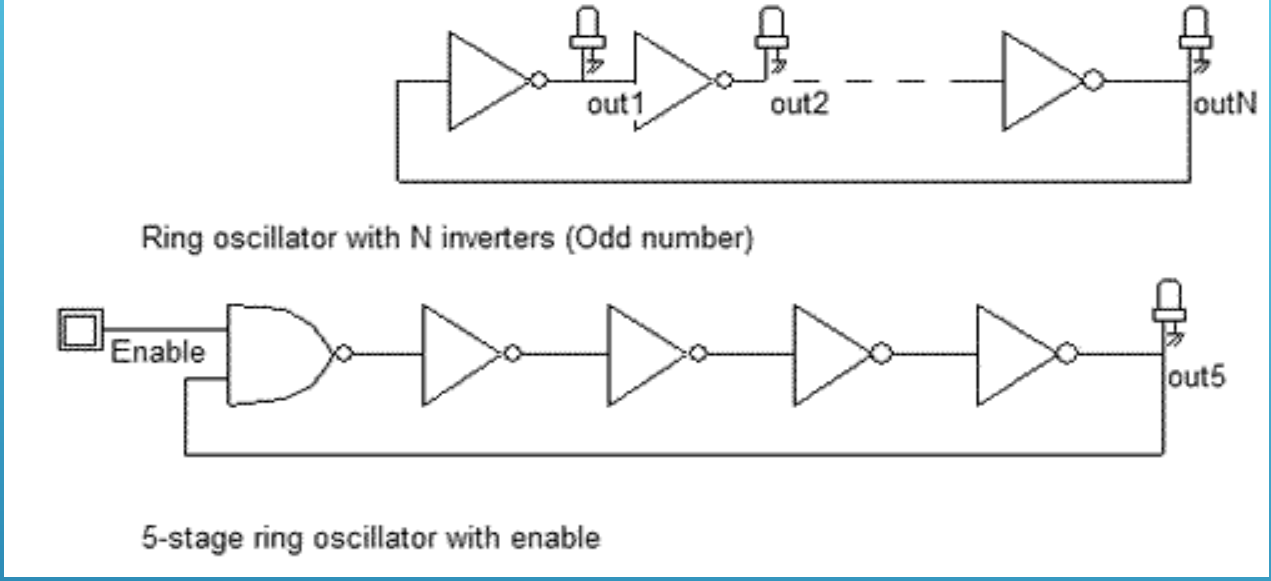
Power delivered to the load

$$P_L = \frac{v_{fund}^2}{2R} = \frac{8V_{DD}^2}{\pi^2 R}$$

$$i_{D,max} = \frac{4}{\pi} \cdot \frac{2V_{DD}}{R} = \frac{8V_{DD}}{\pi R} \qquad v_{DS,max} = 2V_{DD}$$

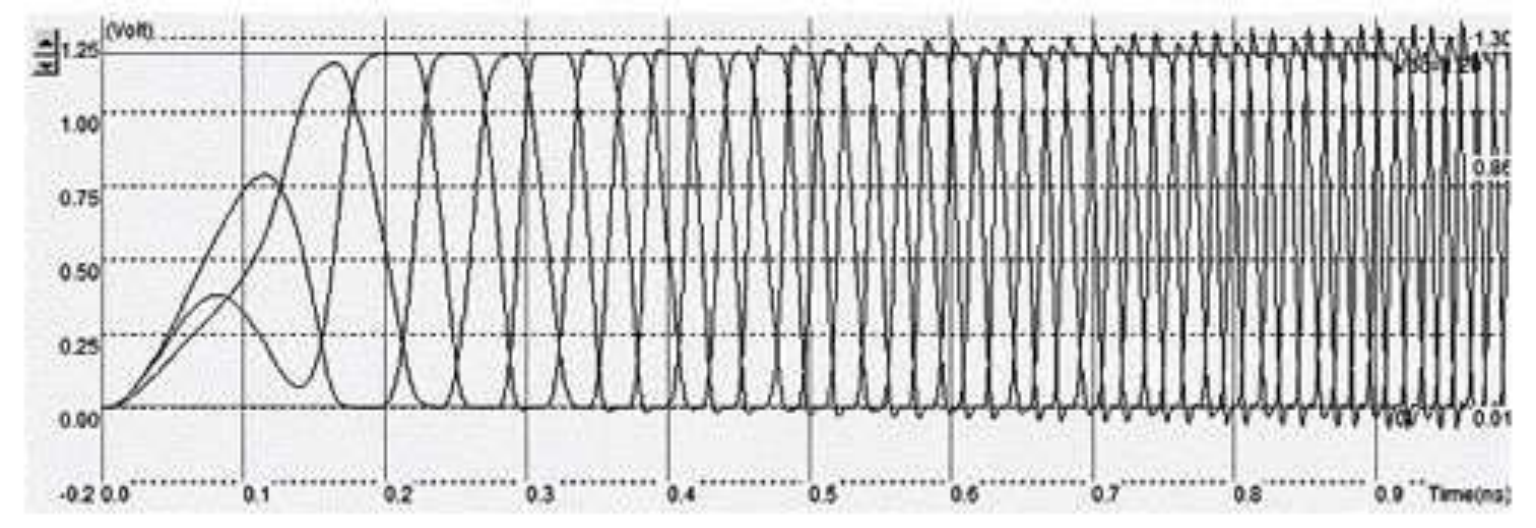
$$P_N = \frac{v_{fund}^2}{2R} = \frac{8V_{DD}^2}{\pi^2 R} / \left(2V_{DD} \cdot \frac{8V_{DD}}{\pi R}\right) = \frac{1}{2\pi} \approx 0.16$$

RING OSCILLATOR



- The ring oscillator is a very simple oscillator circuit, based on the switching delay existing between the input and output of an inverter. If we connect a odd **(even??)** chain of inverters, we obtain a natural oscillation, with a period which corresponds roughly to the number of elementary delays per gate. The usual implementation consists in a series of five up to one hundred chained inverters **(can we obtained oscillation with 1, 3 stages??)** . Usually, one inverter in the chain is replaced by a NAND gate to enable the oscillation.

OSCILLATOR SIMULATION

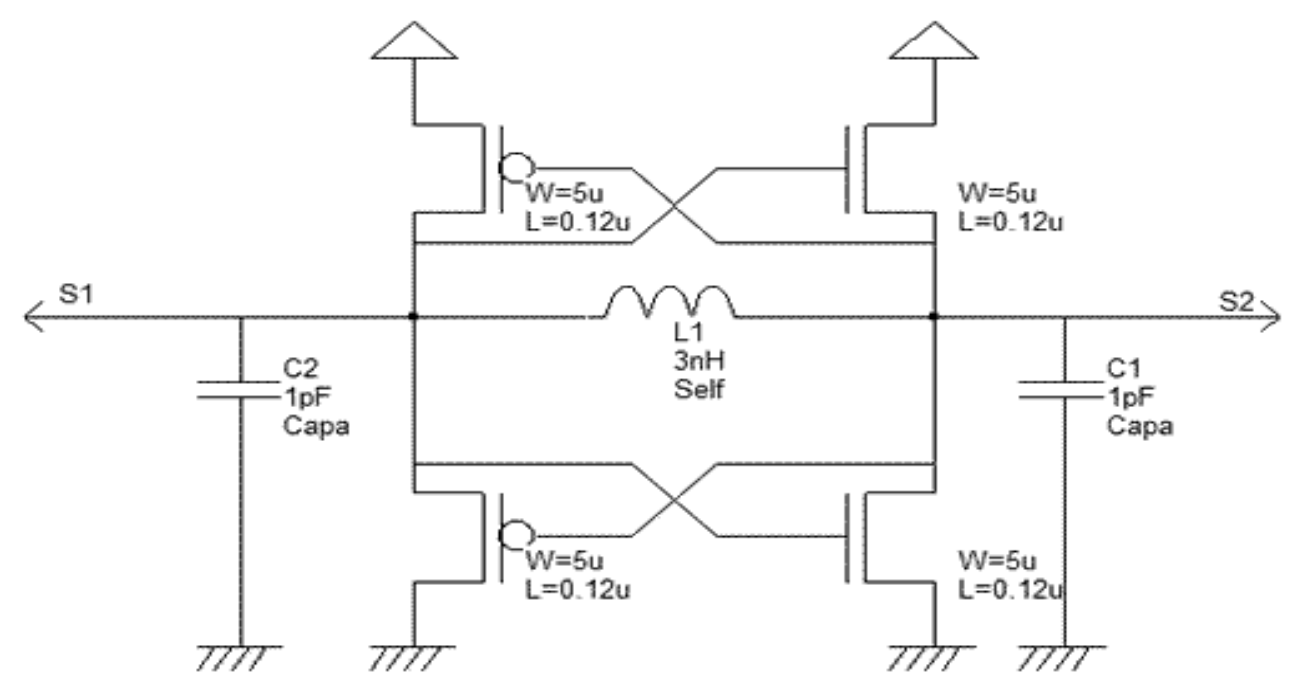


Notice that no clock is assigned in this layout as the oscillation appears naturally, because of an intrinsic instability. The simulation shows the "warm-up" of the inverter circuit followed by a stable frequency oscillation.

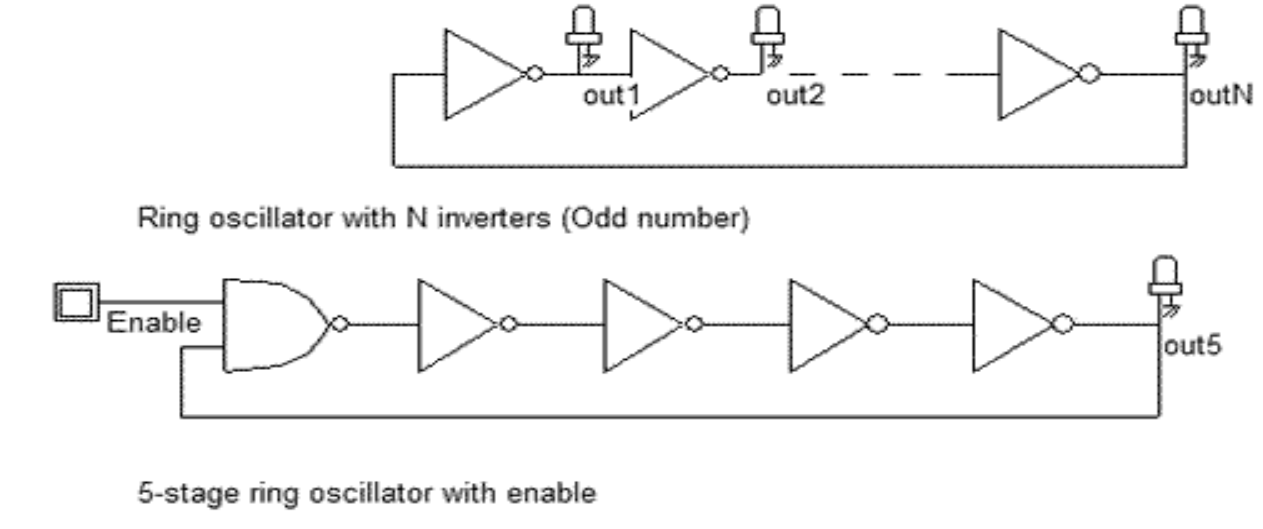
The main problem of this type of oscillator is the very strong dependence of the output frequency with virtually all process parameters and operating conditions: Supply voltage, Temperature and process variation effect on gate switching/propagation delay times .

LC OSCILLATOR

The LC oscillator proposed in this paragraph is not based on the logic delay, as for the ring oscillator, but on the resonant effect of a passive inductor and capacitor circuit. In the following schematic diagram, the inductor *L1* resonates with the capacitor *C1* connected to S1, combined with *C2* connected to *S2*.

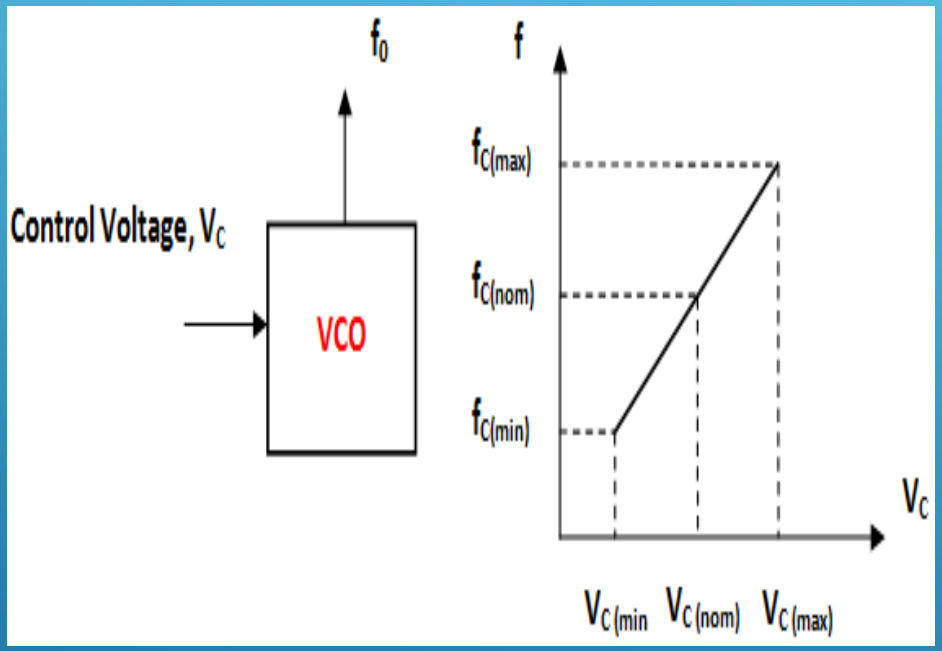


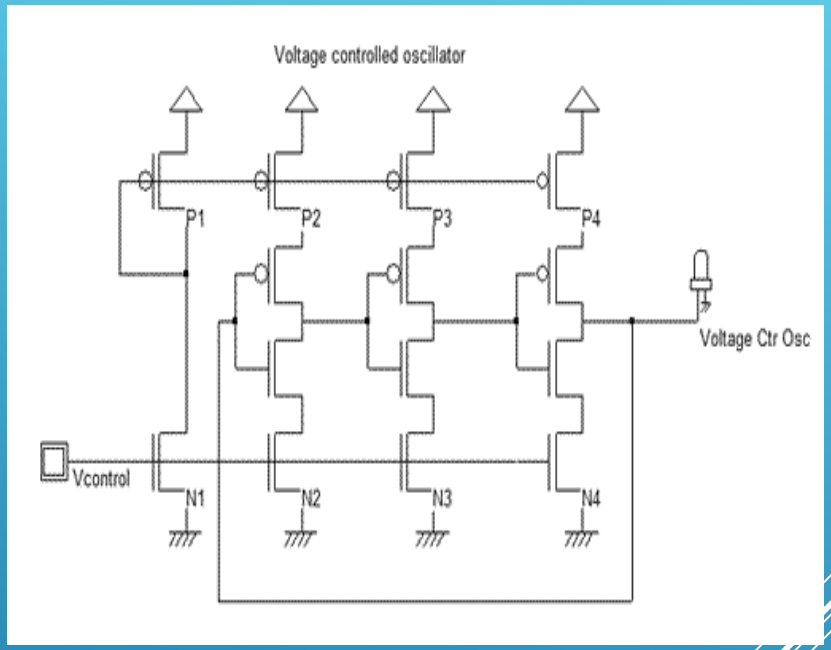
RING OSCILLATOR

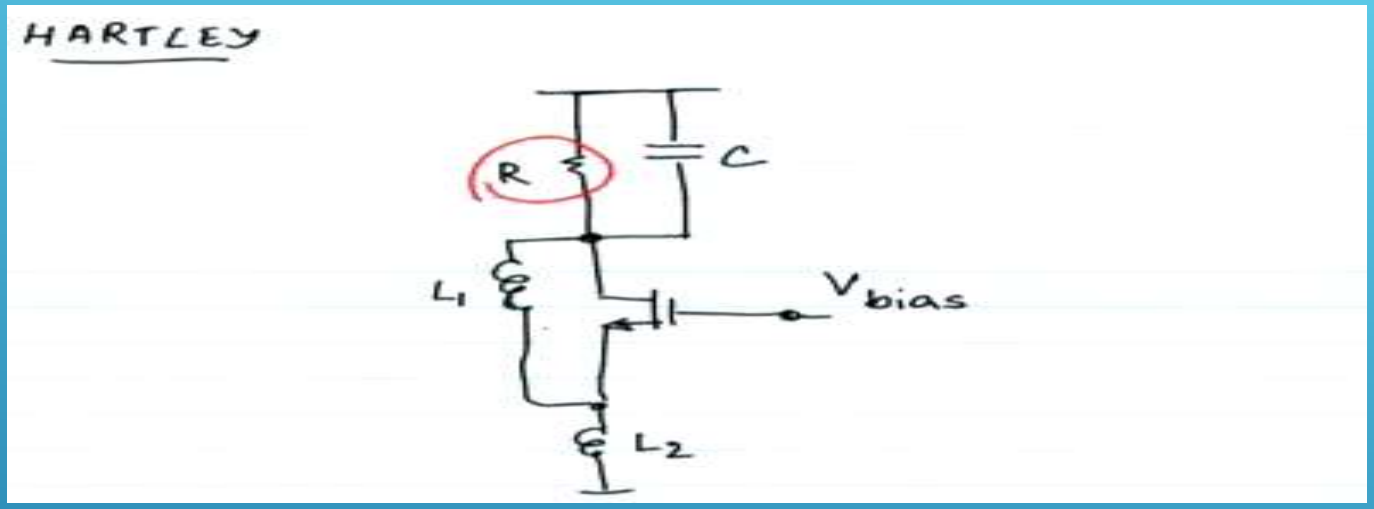


- The ring oscillator is a very simple oscillator circuit, based on the switching delay existing between the input and output of an inverter. If we connect a odd **(even??)** chain of inverters, we obtain a natural oscillation, with a period which corresponds roughly to the number of elementary delays per gate. The usual implementation consists in a series of five up to one hundred chained inverters **(can we obtained oscillation with 1, 3 stages??)** . Usually, one inverter in the chain is replaced by a NAND gate to enable the oscillation.

VCO


f_0
f
Control Voltage, V_C
VCO
$f_{C(max)}$
$f_{C(nom)}$
$f_{C(min)}$
V_C
$V_{C(min}$ $V_{C(nom)}$ $V_{C(max)}$

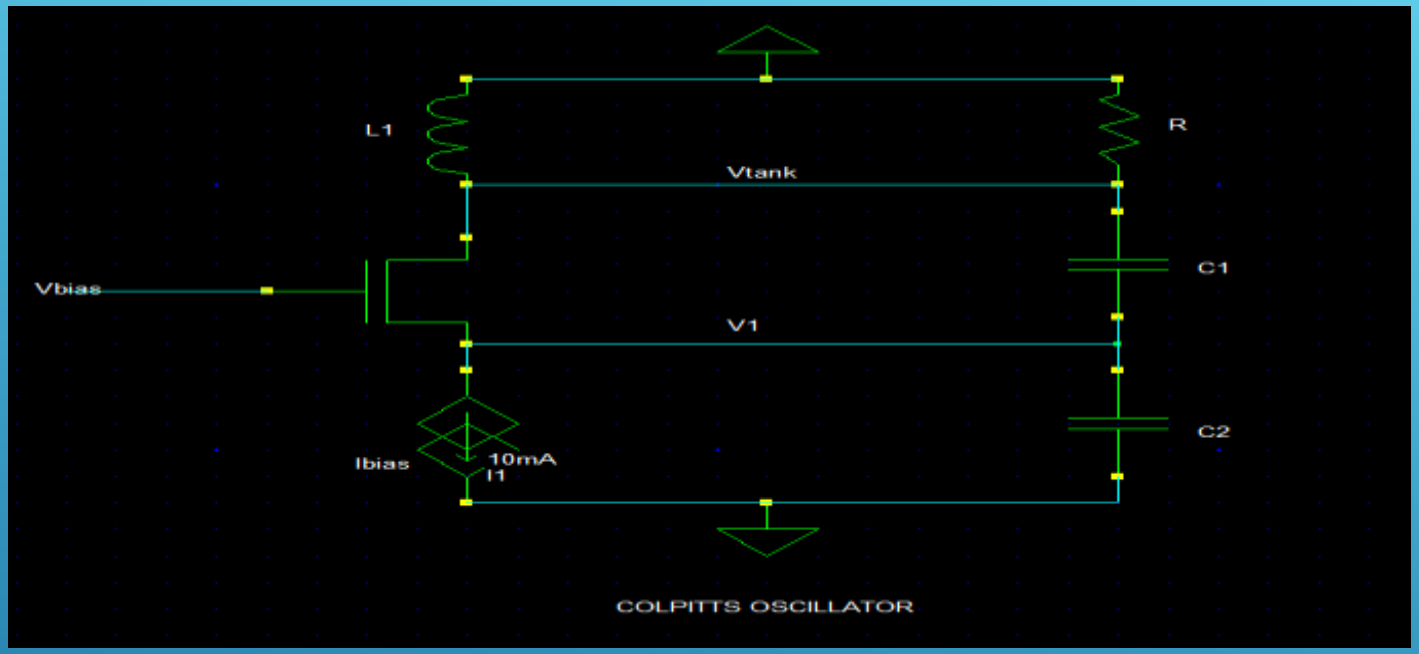

Voltage controlled oscillator
P1
P2
P3
P4
Voltage Ctr Osc
Vcontrol
N1
N2
N3
N4

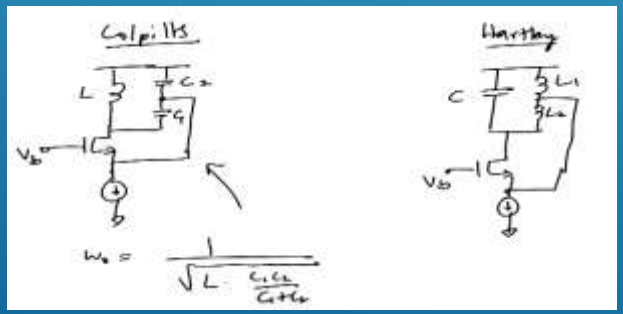


$$L = L_1 + L_2$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

COLPITTS OSCILLATOR





$$C = \frac{C_1 C_2}{C_1 + C_2}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

What is resonator

A *resonator* is a device or system that exhibits resonance or resonant behavior, equencies, called its resonant f thers.

The oscilla gnetic or mechanical

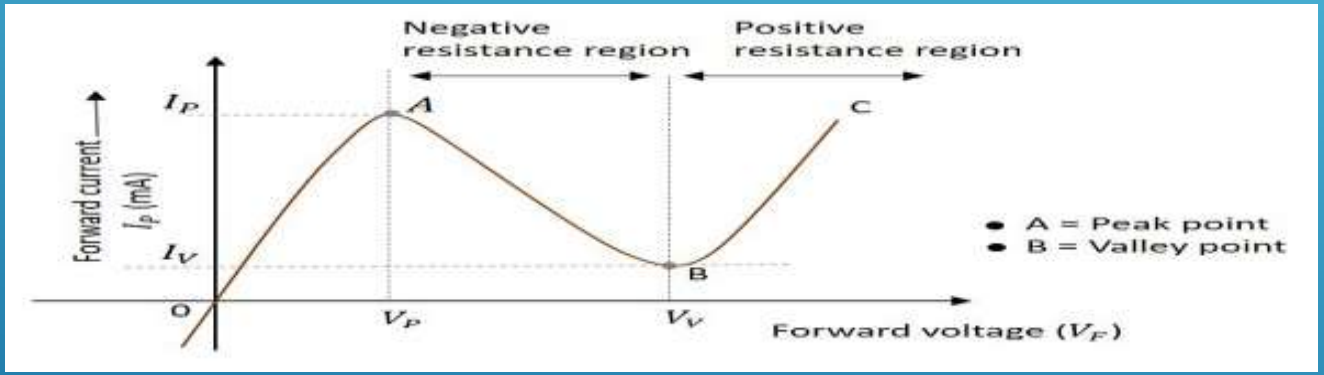
Resonator Technologies

1. Quater-wave resonator
2. Quartz Crystals
3. Surface Acoustic Waves (SAW)

Devices

WHAT IS NEGATIVE RESISTANCE OSCILLATOR

- An **oscillator** that works on **negative resistance**property can termed as a **Negative resistance oscillator**. The term **negative resistance** refers to a condition where an increase in voltage across two points causes a decrease in current.



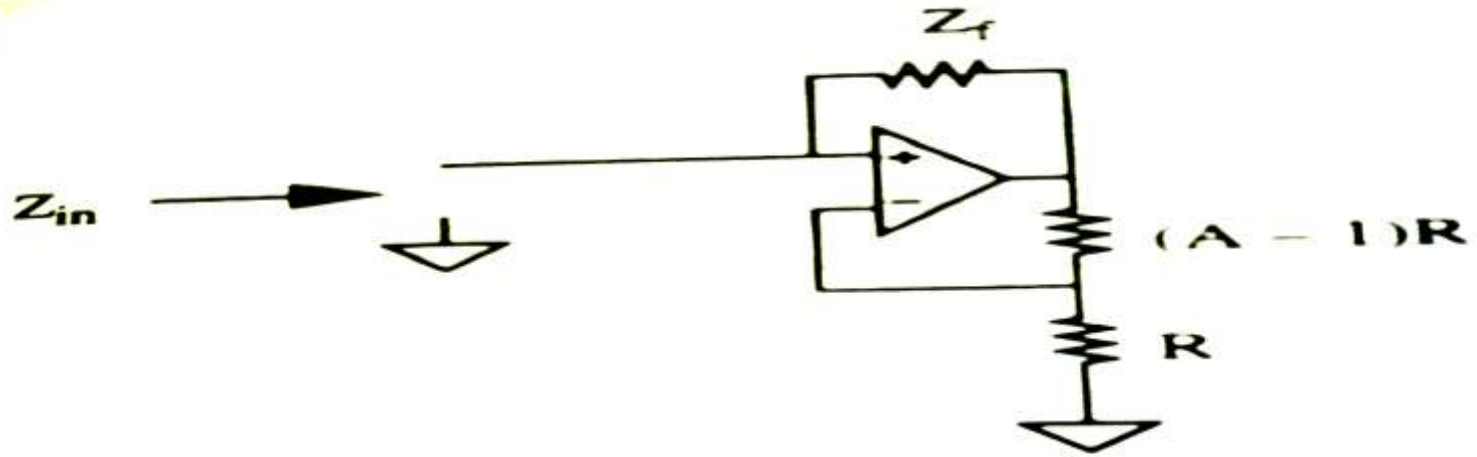


FIGURE 17.33. Generalized impedance converter.

$$Z_{in} = \frac{Z_f}{1 - A}.$$

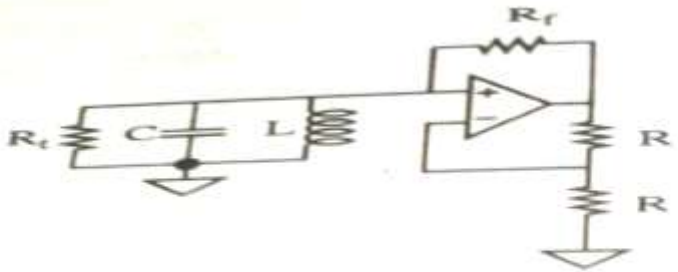


FIGURE 17.34. Negative resistance oscillator.

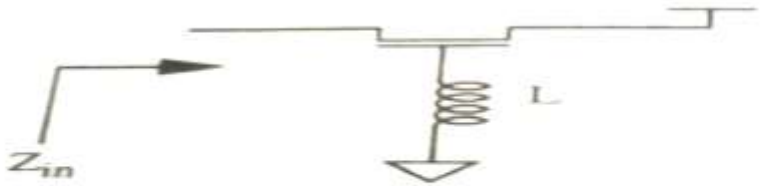


FIGURE 17.35. Canonical RF negative resistance (biasing not shown).

$R_t > R_f$

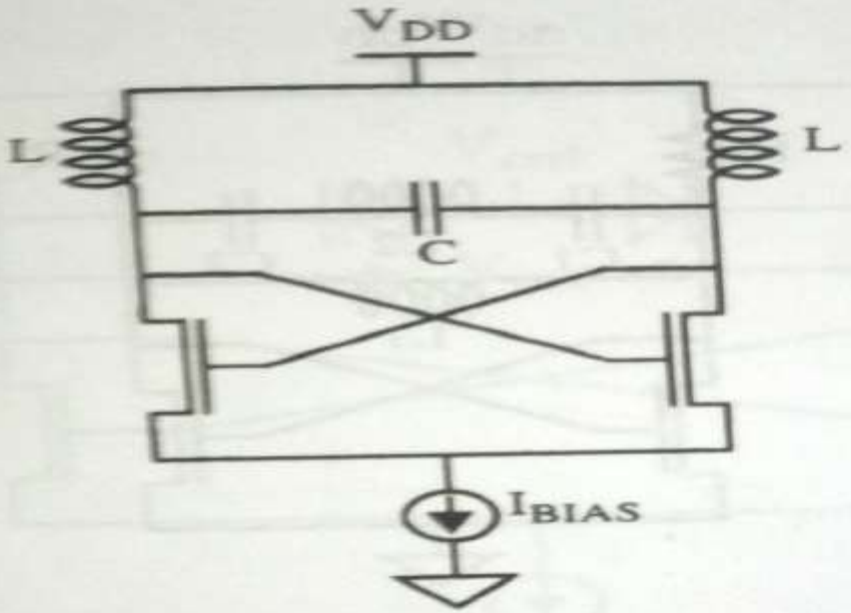
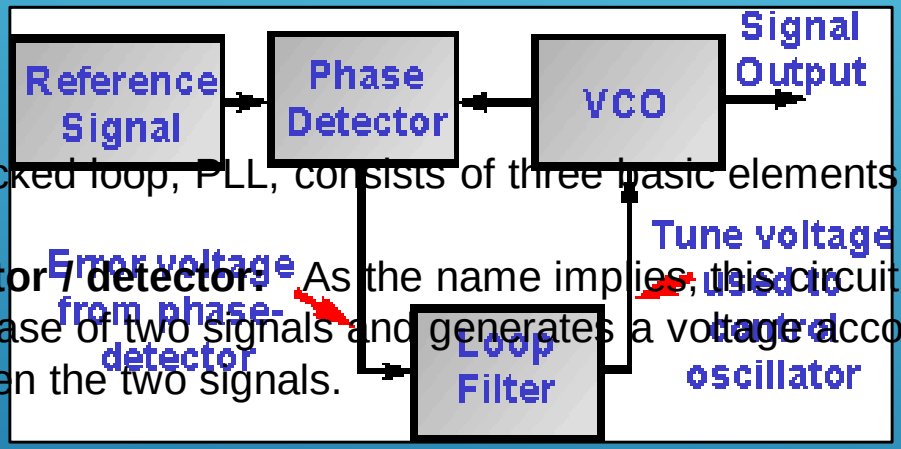


FIGURE 17.36. Simple differential negative resistance oscillator.

PHASE LOCKED LOOP



A basic phase locked loop, PLL, consists of three basic elements:

Phase comparator / detector: As the name implies, this circuit block within the PLL compares the phase of two signals and generates a voltage according to the phase difference between the two signals.

Loop filter: This filter is used to filter the output from the phase comparator in the PLL. It is used to remove any components of the signals of which the phase is being compared from the VCO line. It also governs many of the characteristics of the loop and its stability.

Voltage controlled oscillator (VCO): The voltage controlled oscillator is the circuit block that generates the output radio frequency signal. Its frequency can be controlled over the operational frequency band for the loop

PHASE LOCKED LOOP

In every application, the PLL tracks the phase of the input signal. However, before a PLL can track, it must first reach the phase-locked condition

In general, the VCO center frequency ω_0 differs from the frequency ω_i of the input signal

Therefore, first the VCO frequency has to be tuned to the input frequency by the loop. This process is called *frequency pull-in*

Then the VCO phase has to be adjusted according to the input phase. This process is known as *phase lock-in*

Both the frequency pull-in and phase lock-in processes are parts of acquisition which is a highly nonlinear process and is very hard to analyze

After acquisition the PLL achieves the *phase-locked* condition, where the PLL tracks the input phase. Under this *phase-locked condition*, the VCO frequency is equal to the input frequency

LINEAR PLL

A linear control system model of the phase feedback loop of PLL in the locked state consists of phase detector gain (K_d), VCO gain (K_{vco}/s) and loop filter gain ($F(s)$) divided by the gain of the feedback counter modulus (N) is shown in the figure 7.1.

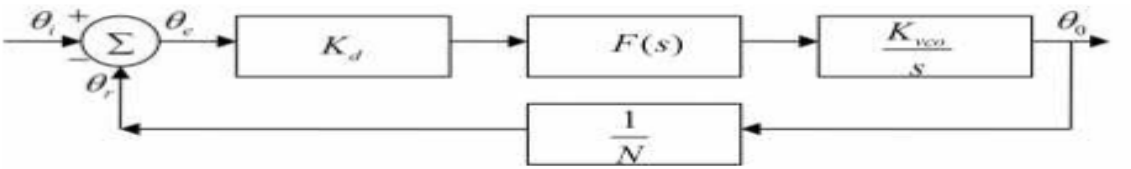


Figure 7.1 Mathematical model of PLL system

A good estimation of loop performance parameters is provided by a linear approximation analysis of mathematical model. The loop parameters such as bandwidth, lock range, settling time and stability of system are found out by the analysis. The analytical equations for a phase transfer function are written using PLL linear model and feedback theory as follows:

$$\text{Forward loop gain: } G(s) = \frac{\theta_0}{\theta_e} = \frac{K_d\ F(s)\ K_{vco}}{s} \tag{7.1}$$

$$\text{Reverse loop gain: } H(s) = \frac{\theta_r}{\theta_0} = \frac{1}{N} \tag{7.2}$$

$$\text{Open loop gain: } G(s).H(s) = \frac{\theta_0}{\theta_i} = \frac{K_d\ F(s)\ K_{vco}}{s\ N} \tag{7.3}$$

$$\text{Closed loop gain: } \frac{\theta_0}{\theta_i} = \frac{G(s)}{1 + G(s)\ H(s)} \tag{7.4}$$

In general loop response for PLL is calculated by equation

$$\frac{\theta_0}{\theta_i} = \frac{K_d K_{vco} F(s)}{s + K_d K_{vco} F(s)} \tag{7.6}$$

Where, θ_0 = the output phase in radians, θ_i = the input phase in radians, K_d = the phase detector gain in volts per radian, K_{vco} = the VCO gain in radians per volt-second

and $F(s)$ = the loop filter transfer function. The loop characteristic of PLL is controlled by a low pass filter. The simplest LPF is a one-pole RC circuit and the first ordered transfer function of LPF is given by eq.(7.7).

$$F(s) = \frac{1}{1 + sRC} \tag{7.7}$$

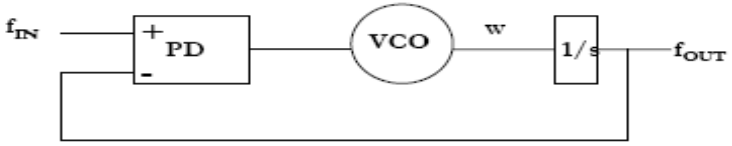
By substituting eq. (7.7) in eq. (7.6), the loop response for second order PLL is as follows.

$$\frac{\theta_0}{\theta_i} = \frac{\frac{K_d K_{vco}}{RC}}{s^2 + \frac{s}{RC} + \frac{K_d K_{vco}}{RC}} \tag{7.8}$$

The standard transfer function second order system is given as

$$T(s) = \frac{s^2}{s^2 + 2s\xi\omega_n + \omega_n^2} \tag{7.9}$$

Basic PLL

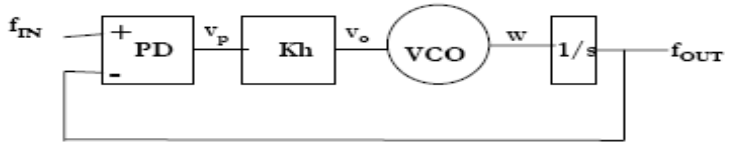


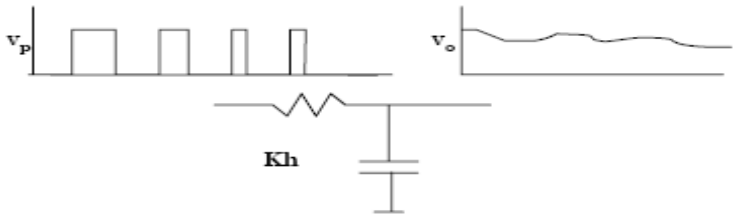
Open loop $\frac{K_d K_v}{s} = \frac{K}{s}$

Closed loop $\frac{1}{1 + s/K}$

That is fine for small signal linear control loop
But large signal(bias) output of PD may not be directly compatible with VCO input.
Need gain/attenuation/shift/filtering: Loop filter

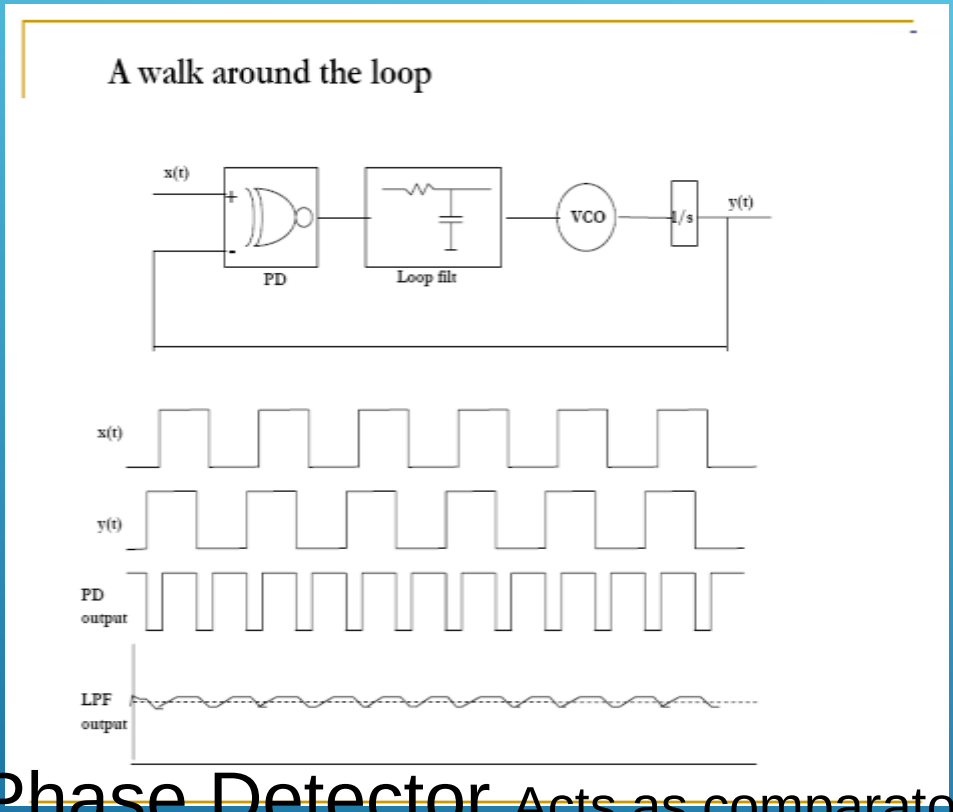
Normally v_p is discrete(like PWM)
Required v_o is steady (DC)
v_p can be converted to v_o by simple LPF

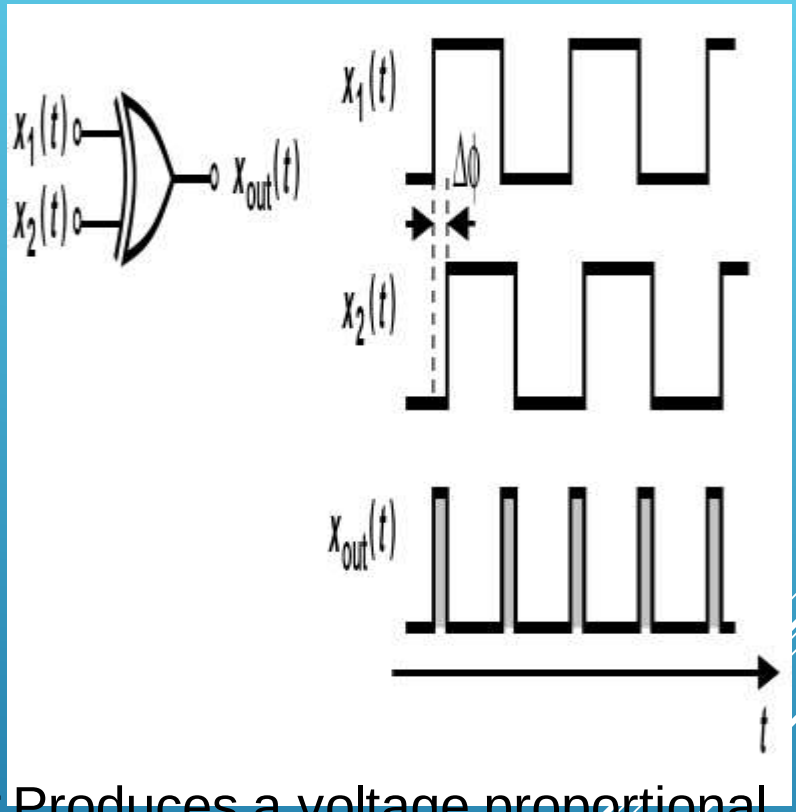




Discrete nature of PD (and v_p) can be treated by continuous linear loop if bandwidth of the loop is within 1/10-th of the frequency of v_p

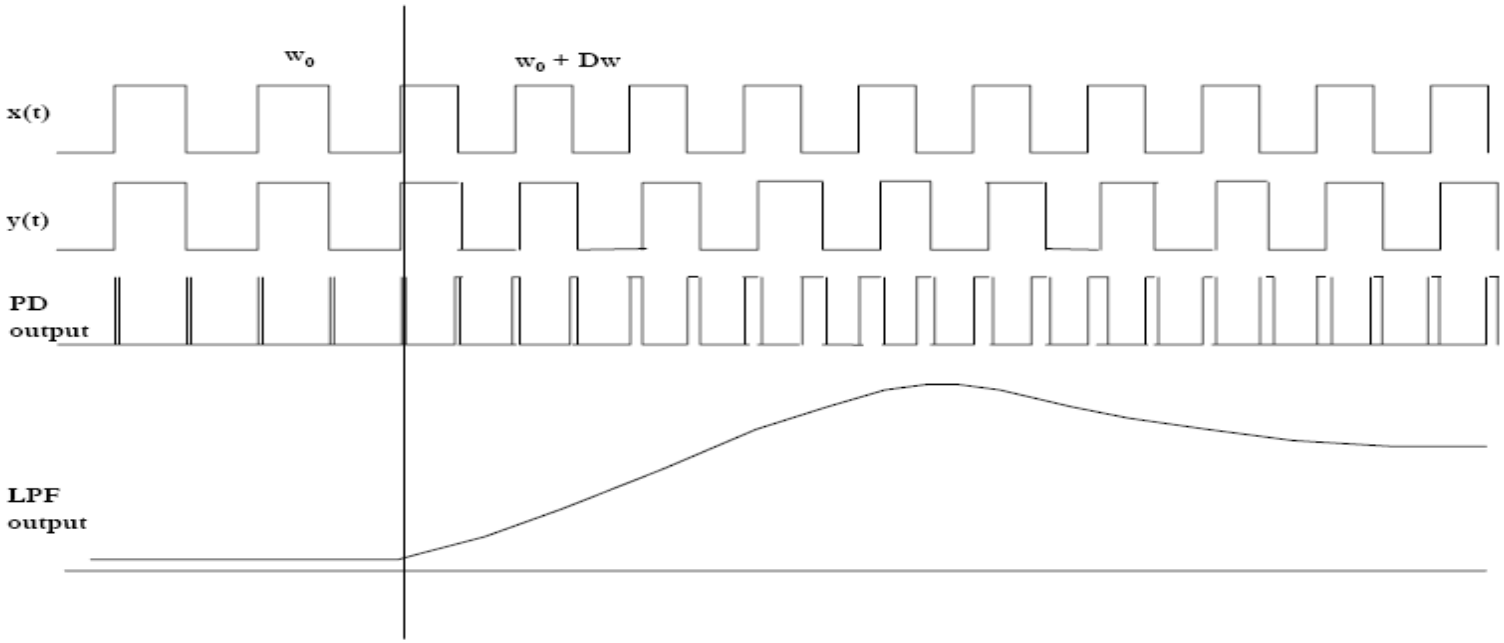
PHASE DETECTOR





Phase Detector Acts as comparator Produces a voltage proportional to the phase difference between input and output signal Voltage becomes a control signal

Frequency step at input

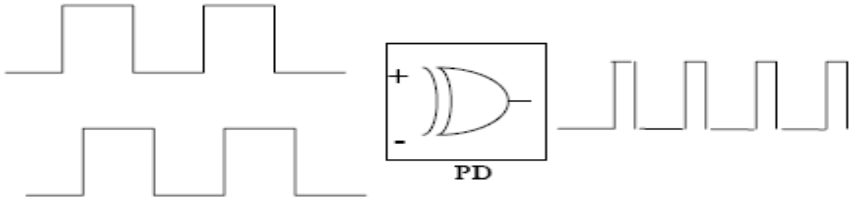


System has memory

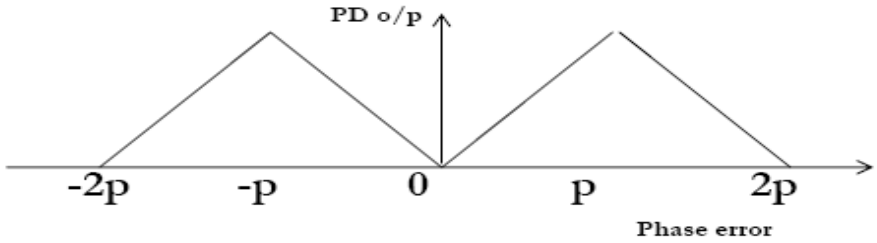
At lock, input and output frequencies are equal

Phase Detector

XOR Phase detector



Simple XOR PD works for a small range of *Df*, for a large range it becomes nonlinear/non-monotonic

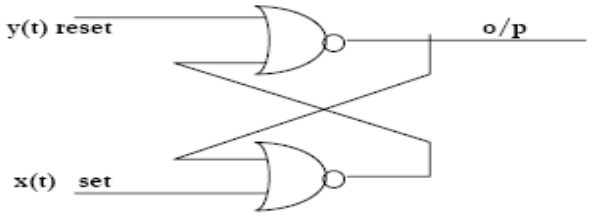


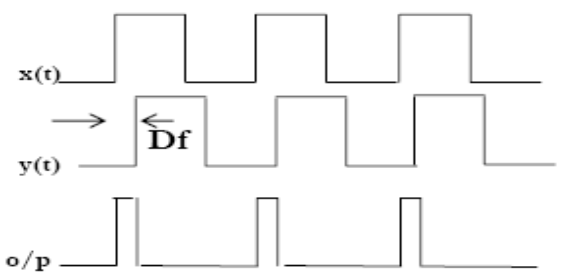
Kd = VDD/p

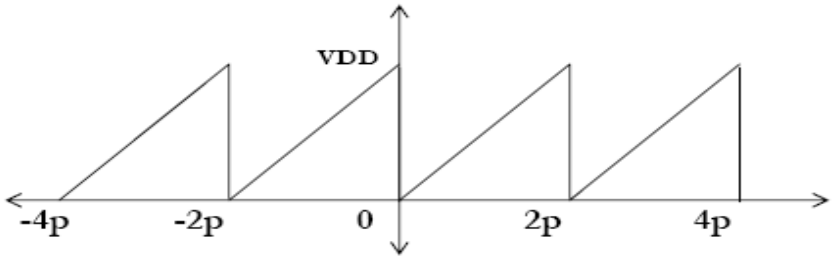
Steady state phase error for most useful range : ?

Phase Detector

Sequential Phase detector (SR flip-flop)



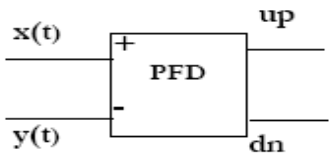


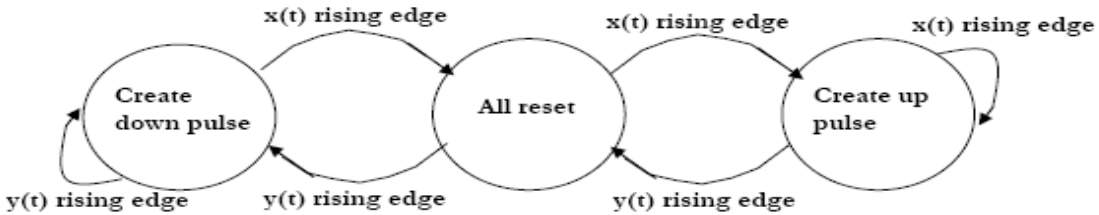


Kd = VDD/2p

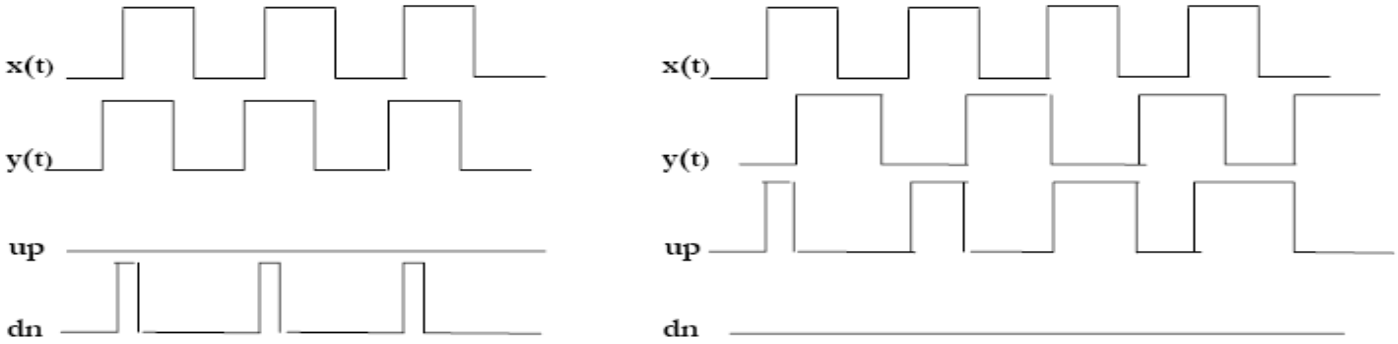
Most useful range offered when Df = p : cannot use for 0 steady state phase error

Phase Frequency Detector (PFD)



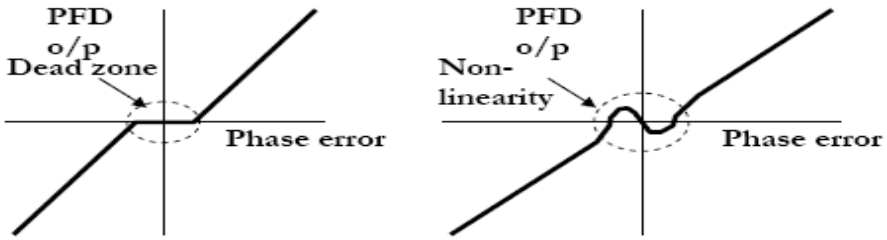


Three-state state machine representation

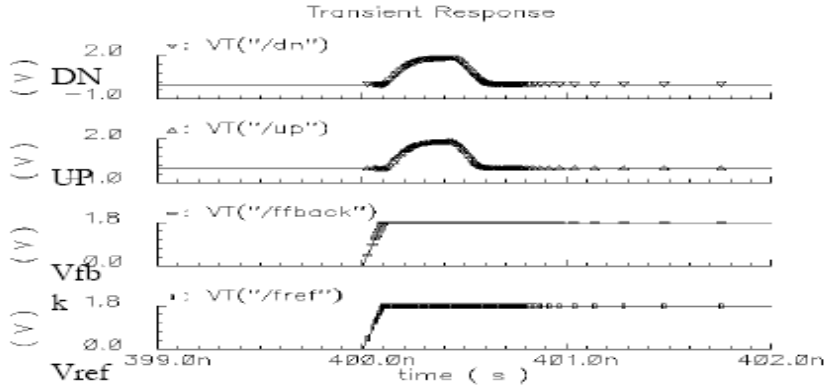


Output UP and DN pulses

Phase Frequency Detector (PFD)



PFD dead zone and non-linearity near zero



Simulated waveform of PFD under lock condition

- Dead zone: phase error below the zero gain region cannot be corrected
- Non-monotonic / non-linear behavior near 0 is also a problem

- Dead zone problem is eliminated by using a certain minimum UP and DN pulse under lock condition

PLL LOOP FILTERS

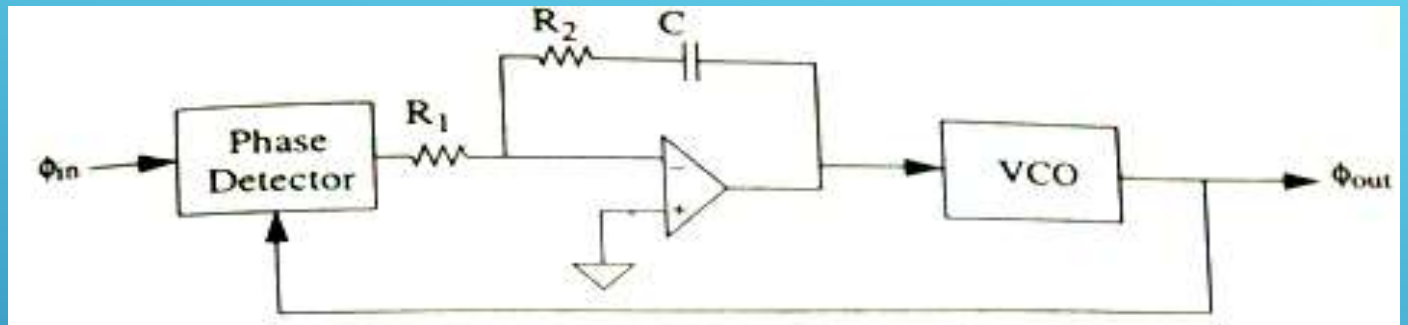
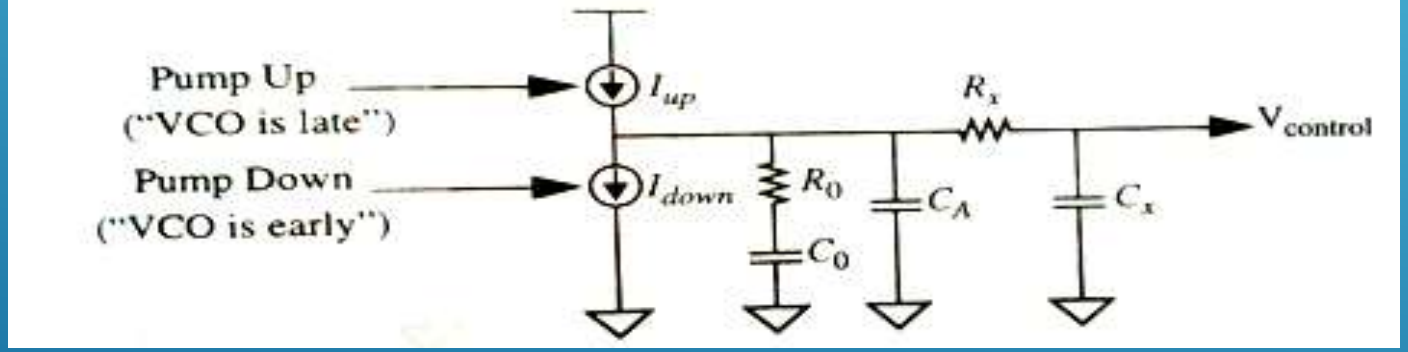


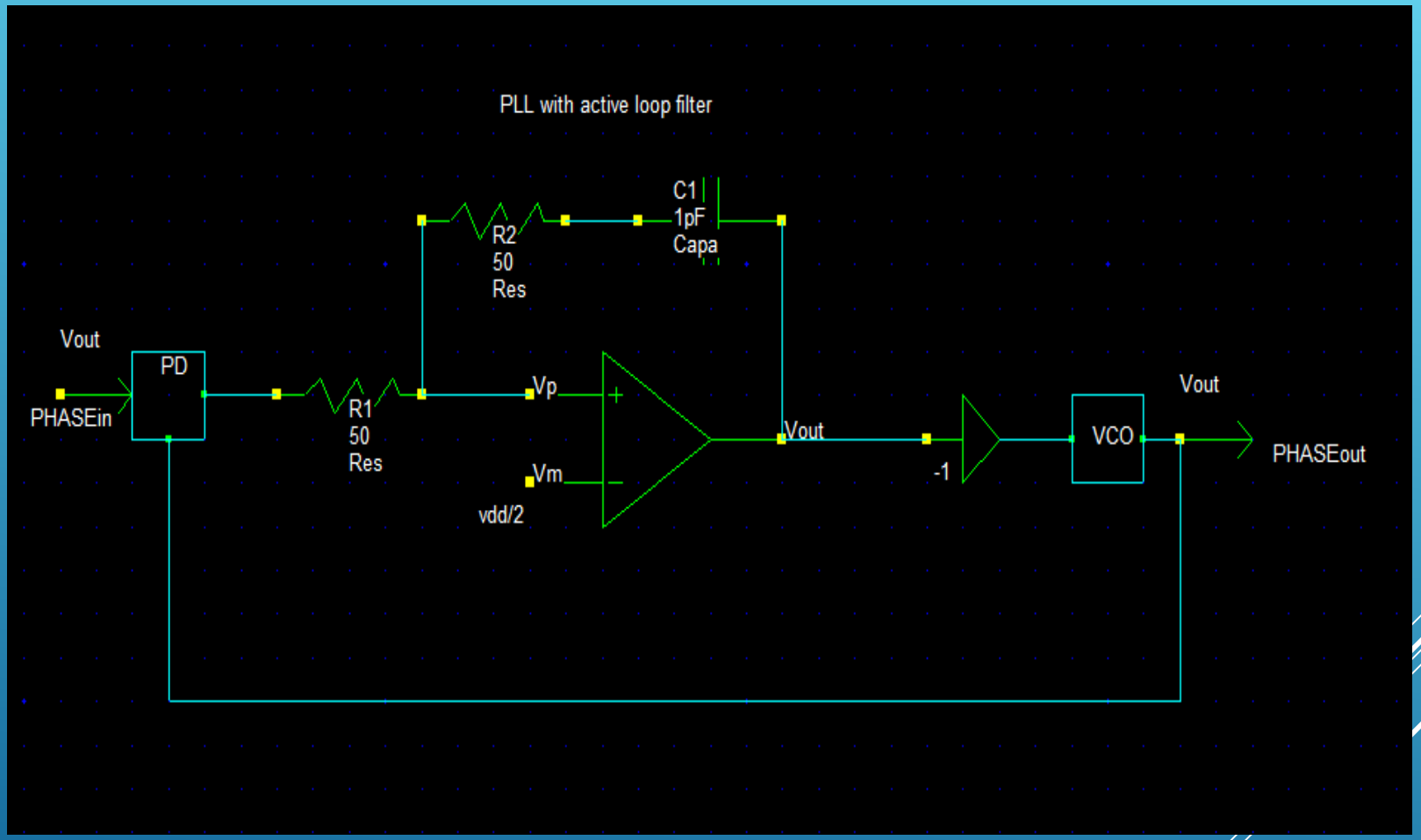
FIGURE 16.29. PLL with typical loop filter.



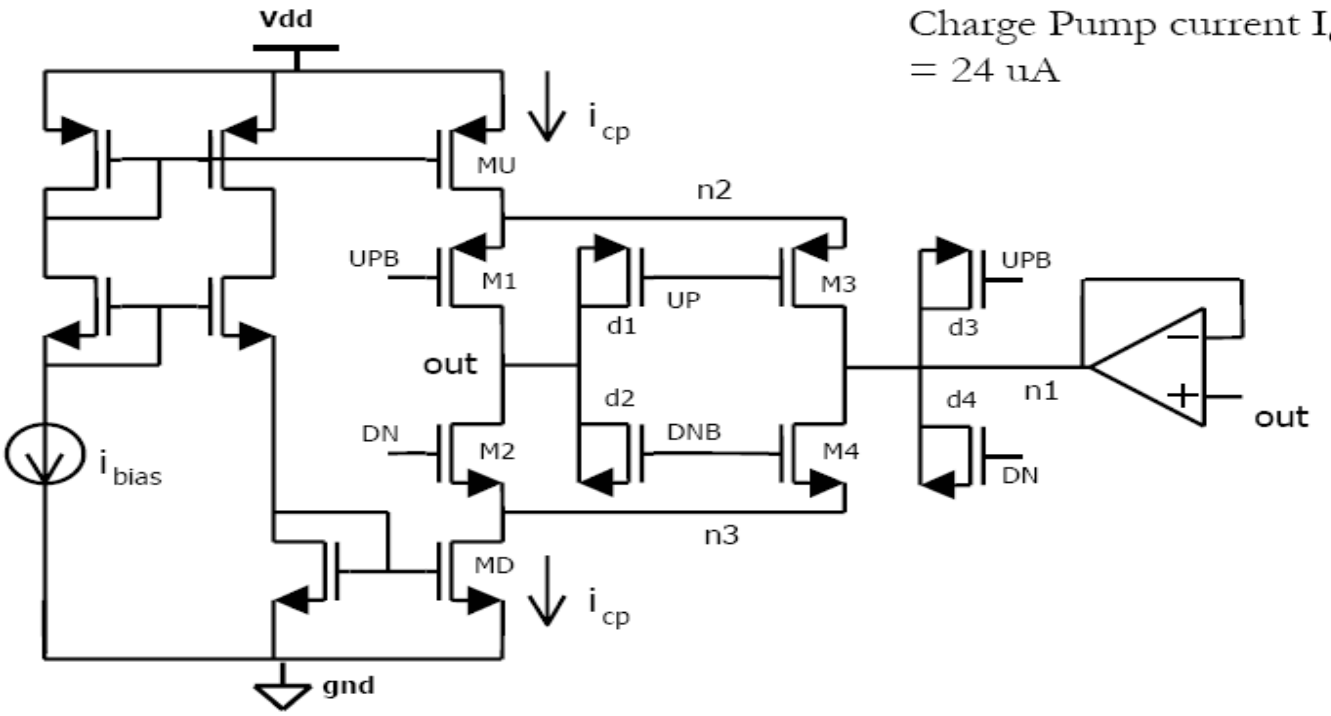
PLL LOOP FILTERS WITH CHARGE PUMP

LOOP FILTER

- Filter
  - Determines dynamic characteristics of PLL
    - Specify Capture Range (bandwidth)
    - Specify Tracking Range
  - Receives signal from Phase Detector and filters accordingly
- The output of the phase detector is filtered by a low-pass loop filter. The filter output voltage $\mathbf{V_o}$ controls the frequency of the VCO.


PLL with active loop filter
C1
1pF
Capa
R2
50
Res
Vout
PD
PHASEin
R1
50
Res
Vp
Vm
vdd/2
Vout
-1
VCO
Vout
PHASEout

Charge Pump (CP)



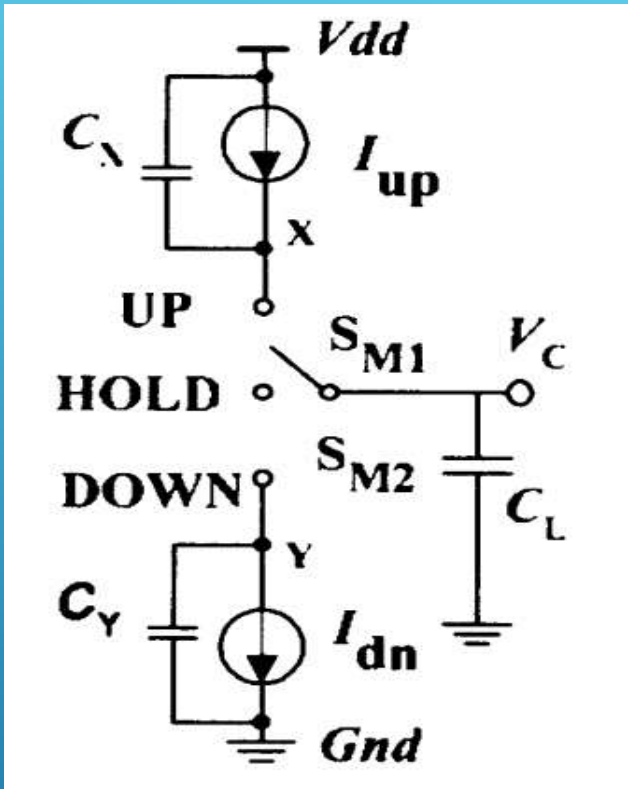
Charge Pump current I_{CP} = 24 uA

CHARGE PUMP

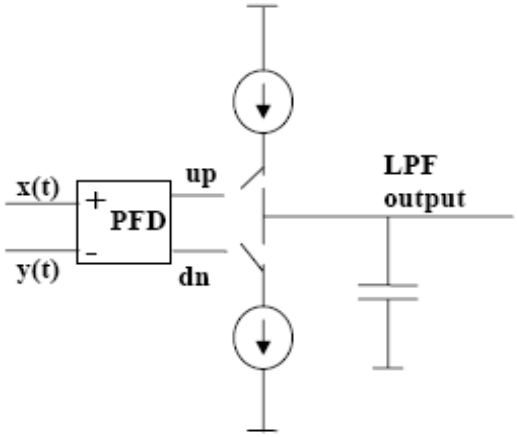
- **UP state:** the switch SM1 is on and SM2 is off; the load capacitor CL is charged by Iup and the voltage Vc rises.
- **DOWN state:** SM1 is off and SM2 is on, which causes CL to be discharged by Idn and Vc falls.
- **HOLD state:** SM1 and SM2 are both off, then no current flows into CL and Vc is held, which means that the PLL is locked.

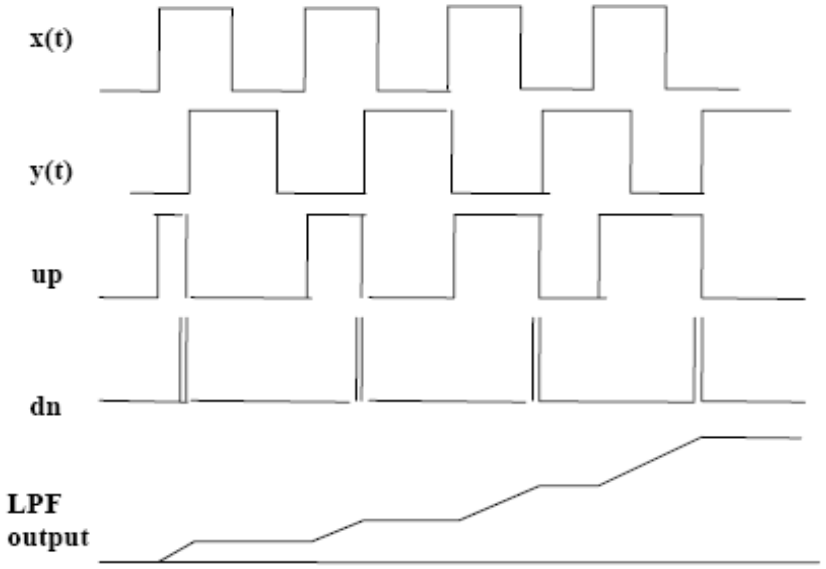
In ideal case, SM1 and SM2 will never be on at the same time.

- SM1 and SM2 are usually implemented using PMOS and NMOS devices respectively

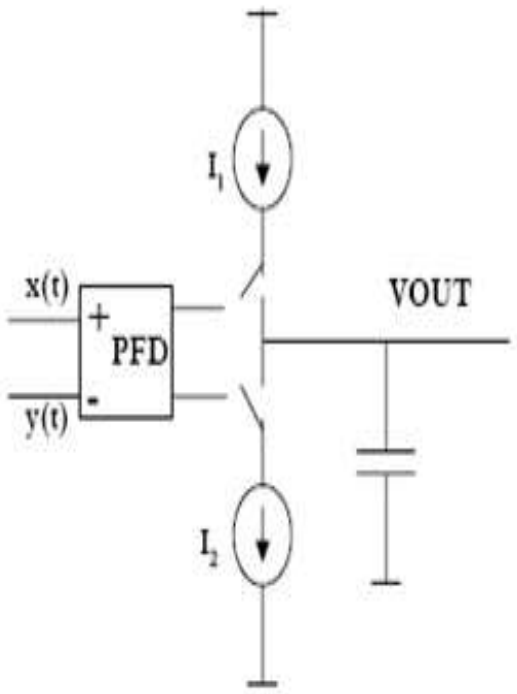


Phase-Frequency Detector + Charge pump





Phase-Frequency Detector + Charge pump



Status of UP/DOWN pulses is converte
to a DC current to get PFD + CP gain
characteristic.

average charging current = $(t_1/T)*I_1$

average discharging current = $(t_2/T)*I_2$

t_1: on time of UP pulse

t_2: on time of DN pulse

T: time period

THANK YOU