	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-1** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

1. MOSFET is a [ ]

(a) Current controlled device (b) voltage controlled device (c) both (d) none

2. In MOSFET which region is used for amplification [ ]

(a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

3. CMOS Logic levels [ ]

(a) 0-2.0v & 4.0-5.0v (b) 0-1.5v & 3.5-5.0v (c) 0-2.3v & 3.7-5.0v (d) 0-1.9v & 3.1-5.0v

4. MOSFET is a [ ]

(a) Square law device (b) exponential device (c) constant device (d) none of the above

5. Input impedance of MOSFET is [ ]

(a) Very high (b) high (c) very low (d) low

6. Which of the following statements is incorrect? [ ]

(a)ECL has high power consumption.(b) ECL is widely used in high-speed applications.

(c)ECL is one of the fastest forms of electronic logic.(d)ECL suffers from low noise immunity.

7. RCTL stands for_____

8. Fastest logic gate family is [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

9. Which of the following family not belongs to bipolar logic gate families [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

10. The logic gate which has highest fan-out is [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

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11. VHISC is an acronym for _____

12. The HDL compiler analyzes our code for [ ]

(a)Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

13. A VHDL Entity gives [ ]

(a)External behavior or declaration of modules (b) Internal behavior or structure

(c)Both (d) None of the above

14. The process which used to verify that the circuit work as desired is called[ ]

(a)Testing (b) Compilation (c) Simulation (d) Synthesis

15. DTL stands for _____

16. The Structural style of model consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

17. The Behavioral style of modeling consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

18. "A component instantiated in structural description must first be declared using a Component declaration". The statement is (TRUE/FALSE)

19. A Component declaration declares [ ]

(a) Name of the component (b) Interface of the component

(c) Both (a) and (b) (d) None of the above

20. The Dataflow modeling consists of [ ]

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	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-2** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** | **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

1. CMOS logic circuit operates from a_____ power supply

2. In PMOS as Vgs (gate to source voltage) decreases Rds (drain to source resistance

(a) Increases (b) Decreases(c) Remains constant (d) none of the above [ ]

3. In NMOS as Vgs(gate to source voltage) increases Rds(drain to source resistance [ ]

(a) Increases (b) Decreases(c) Remains constant (d) none of the above

4. In CMOS as fan-in increases on resistance of the series transistors [ ]

(a) Increases (b) Decreases(c) Remains constant (d) none of the above

5. Which of the following topic not comes under static behavior of the CMOS [ ]

(a) Fan out (b) logic levels (c) noise margins (d) Transition time

6. HTL is a modified form of [ ]

(a) DCTL (b) DTL (c) TTL (d) ECL

7. Fastest logic gate family is [ ]

(a) RTL (b) DTL (c) ECL (d) CMOS

8. Bipolar junction transistor acts as a _____

9. The voltage levels of ECL gate [ ]

(a) -1.8v and 0.8 (b) -0.8 and 1.8 (c) -2.3v and 3.7 (d) -1.9v and 3.1

10. In Bipolar Junction Transistors which region is used for amplification [ ]

(a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

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MID – I OBJECTIVE PAPER		**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
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(a) Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

12. A VHDL Architecture gives [ ]

(a)External behavior or declaration of modules (b) internal behavior or structure

(c) Both (d) None of the above

13. The buffer mode specifies [ ]

(a) Input of the entity (b)Output of the entity

(c)Either input or output (d)None of the above

14. The in out mode specifies [ ]

(a) Input of the entity (b) Output of the entity

(c) Either input or output (d)None of the above

15. In type STD-ULOGIC 'U' stands for _____

16. The Interface of the component specifies [ ]

(a) Mode of the port (b) Type of the port (c) Both (a) and (b) (d) None of the above

17. "In concurrent statements the ordering is most important".

The statement is

(TRUE/FALSE)

18. Which of the following statement come under behavioral modeling [ ]

(a) Wait Statement (b) If Statement (c) Case Statement (d) All the above

19. The Dataflow modeling consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

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	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-3** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** / **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

1. Which of the following topic not comes under static behavior of the CMOS? [ ]

   (a) Fan out (b) logic levels (c) noise margins (d) Transition time

2. The ability of an output to charge and discharge the stray capacitance is sometimes called _____

3. Compare to other logic families CMOS fan-out is [ ]

   (a) More (b) less (c) equal (d) less than or equal

4 .CMOS logic gates has [ ]

(a) less power consumption (b) high fan-out (c) low noise margin (d) both (a) and (b)

5. The amount of time that the output of logic circuit takes to change from one state to another is called the_____

6. HTL is a modified form of [ ]

   (a) DCTL (b) DTL (c) TTL (d)ECL

   10. DCTL stands for _____

7. Which of the following family not belongs to bipolar logic gate families [ ]

   (a)RTL (b)DTL (c)ECL (d)CMOS

8. Fastest logic gate family is [ ]

   (a)RTL (b)DTL (c)ECL (d)CMOS

9. The logic gate which has highest fan-out is [ ]

   (a)RTL (b)DTL (c)ECL (d)CMOS

10. When the current flows into TTL output in LOW state, the output is said to be _____

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-3** **Sign of the Invigilator**
	MID – I OBJECTIVE PAPER	**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** / **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

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3. Compare to other logic families CMOS fan-out is [ ]

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11. The signals which are defined within the Package are [ ]

(a) global signals (b) local signals (c) Both (d)none

12.The VHDL Compiler automatically creates and uses a library named [ ]

(a) User defined library (b) Work library (c) STD-ULOGIC (d) Enumerated type

13. In type STD-ULOGIC 'X' stands for _____

14. The HDL compiler analyzes our code for [ ]

(a) Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

15. The buffer mode specifies [ ]

(a) Input of the entity (b) Output of the entity

(c) Either input or output (d) none of the above

16. The Interface of the component specifies [ ]

(a) Mode of the port (b) Type of the port (c) Both (a) and (b) (d) None of the above

17. "In concurrent statements the ordering is most important".

The statement is

(TRUE/FALSE)

18. Which of the following statement come under behavioral modeling [ ]

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19. The Dataflow modeling consists of [ ]

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	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-4** **Sign of the Invigilator**
	MID – I OBJECTIVE PAPER	**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** / **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

1. Which of the following is sequential statement [ ]

(a) NULL (b) LOOP (c) EXIT (d) All the above

2. The VHDL Simulator is used to [ ]

(a) To correct syntax errors (b) To identify semantic errors

(c) To observe the operation (d) To identify syntax errors

3. Which of the following statements not come under Dataflow modeling [ ]

(a) Case Statement (b) Block statements

(c) Concurrent assertion statements (d) Selected signal assignment statements

4. A Component declaration declares [ ]

(a) Name of the component (b) Interface of the component

(c) Both (a) and (b) (d) None of the above

5. The Structural style of model consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

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6. HTL is a modified form of [ ]

(a) DCTL (b) DTL (c) TTL (d) ECL

7. Fastest logic gate family is [ ]

(a) RTL (b) DTL (c) ECL (d) CMOS

8. Bipolar junction transistor acts as a _____

9. The voltage levels of ECL gate [ ]

(a) -1.8v and 0.8 (b) -0.8 and 1.8 (c) -2.3v and 3.7 (d) -1.9v and 3.1

10. In Bipolar Junction Transistors which region is used for amplification [ ]

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	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-4** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** / **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
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14. The process which used to verify that the circuit work as desired is called [ ]

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15. DTL stands for _____

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Code: 15A04504 SET 1 R15

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

Department of ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech III Year I Sem (R15) First Mid-term Examinations, 09 September, 2019

DIGITAL SYSTEM DESIGN

Time: 90 minutes Max.Marks:30

Part – A

(Compulsory Question)

Answer the following: (5 x 2 = 10 Marks)

1. Explain about the CMOS Logic MOS Transistors?
2. Difference between Schottky transistor and Standard TTL?
3. Briefly describe the program structure of VHDL?
4. What are the various types of objects in VHDL and give the necessary examples?
5. How schottky transistors are formed and state its use?

Part-B

Note: Answer **TWO** Questions; Either 2nd Question or 3rd Question & Either 4th Question or 5th question

2a) Explain how CMOS_TTL interfacing can be achieved. Give the input and output levels of voltages and explain the same? 5M

2b) Explain about basic CMOS Inverter Circuit with functional behavior and switch model operation? 5M

OR

3a) Design a 4-input CMOS AND-OR-INVERT gate? Explain the circuit with the help of logic diagram and function table? 4M

3 b) Draw the circuit diagram of two input 10K ECL OR/NOR gate and explain its operation? 6M

4a) Discuss the steps in VHDL design flow. 6M

4b) Explain the difference in program of VHDL and any other procedural language. Give example? 4M

OR

5a) Design the logic circuit and write the data-flow style VDHL program for the following functions F(Y)= $\sum_{A,B,C,D}(1,4,5,7,9,11,12,13,1,5)$ 6M

5b) Design the logic circuit and write a structural-flow style VHDL program for the following function? F(Q)=$\prod_{P,R,R,S}(1,3,4,5,6,7,9,12,13,14)$? 4M

Code: 15A04504 SET 2 R15

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

Department of ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech III Year I Sem (R15) First Mid-term Examinations, 09 September, 2019

DIGITAL SYSTEM DESIGN

Time: 90 minutes Max.Marks:30

Part – A

(Compulsory Question)

Answer the following: (5 x 2 = 10 Marks)

1. Explain how a CMOS device is destroyed?
2. Explain about positive ECL (PECL)?
3. What are the constants of objects in VHDL and write the syntax with necessary examples?
4. Explain about the functions of VHDL with syntax and example
5. Mention the important characteristics of digital IC's?

Part-B

Note: Answer **TWO** Questions; Either 2nd Question or 3rd Question & Either 4th Question or 5th question

2a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation? 6M

2b) What is interfacing? Explain interfacing between low voltage CMOS logic, can it tolerate input voltage greater than $v_{cc,}$ if not explain? 4M

OR

3a) Explain how CMOS_TTL interfacing can be achieved. Give the input and output levels of voltages and explain the same? 4M

3b) Draw the circuit diagram of two inputs LS_ TTL NOR gate and explain the functional behavior? 6M

4a) Explain structural design elements of VHDL with example? 6M

4b) Write a behavioral style VHDL program for the following functions 4M

a) $F(S)=A+B+C^1$
b) $F(C_0)= AB+AC^1+BC^1$

OR

5a) Design the logic circuit and write a data-flow style VHDL program for the following function? $F(X)= \sum_{A,B,C,D}(1,5,6,7,9,13) + D(4,15)$ 4M+6M

5b) what are the various types of objects in VHDL and give the necessary examples?

Code: 15A04504 SET 3 R15

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

Department of ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech III Year I Sem (R15) First Mid-term Examinations, 09 September, 2019

DIGITAL SYSTEM DESIGN

Time: 90 minutes Max.Marks:30

Part – A

(Compulsory Question)

Answer the following: (5 x 2 = 10 Marks)

1. Explain about CMOS Logic. Sketch 2-input CMOS NAND gate .Explain their operation?
2. Explain the following terms with reference to CMOS logic? i. Logic Levels ii. DC Noise margin with typical i/p & o/p transfer characteristics of a CMOS Inverter
3. What is pure function and impure function? Explain with example?
4. Explain about the procedures in VHDL and write its syntax?
5. Write the comparison between TTL, CMOS, and ECL

Part-B

Note: Answer **TWO** Questions; Either 2nd Question or 3rd Question & Either 4th Question or 5th question

2a) Explain how CMOS_TTL interfacing can be achieved. Give the input and output levels of voltages and explain the same? 6M

2b) Draw the circuit diagram of two inputs LS_ TTL NOR gate and explain the functional behavior? 4M

OR

3a) Draw the resistive model of a CMOS inverter circuit and explain circuit behavior with resistive loads for LOW and HIGH outputs? 4M

3b) What is interfacing? Explain interfacing between low voltage CMOS logic, can it tolerate input voltage greater than $v_{cc,}$ if not explain? 6M

4a) Explain Behavioral design elements of VHDL? 4M

4b) Design a logic circuit to detect prime number of a 4-bit input? Write the structural VHDL program for the above design? 6M

OR

5a) Explain the use of packages. Give syntax and structure of a package in VHDL

5b)Design the logic circuit and write a data-flow style VHDL program for the following function? F(X)= $\sum_{A,B,C,D}(1,5,6,7,9,13) + D(4,15)$ 5M+5M

Code: 15A04504 SET 4 R15

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

Department of ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech III Year I Sem (R15) First Mid-term Examinations, 09 September, 2019

DIGITAL SYSTEM DESIGN

Time: 90 minutes Max.Marks:30

Part – A

(Compulsory Question)

Answer the following: (5 x 2 = 10 Marks)

1. Explain about the following factors consider in TTL/CMOS interfacing
   a) Noise margin b)Fan out c) capacitive load
2. Explain about positive ECL (PECL)?
3. Explain how a CMOS device is destroyed?
4. Draw the two input ECL OR/NOR Gate and explain the operation with functional table and truth table?
5. What is High Threshold Logic?

Part-B

Note: Answer **TWO** Questions; Either 2nd Question or 3rd Question & Either 4th Question or 5th question

2a) Explain about basic CMOS Inverter Circuit with functional behavior and switch model operation? 5M

2b) Compare HC, HCT, VHC and VHCT CMOS logic families with the help of output specifications with VCC from 4.5V to 5.5V? 5M

OR

3a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation 5M

3b) What is interfacing? Explain interfacing between low voltage CMOS logic, can it tolerate input voltage greater than vcc, if not explain? 5M

4a) Design a logic circuit to detect prime number of a 5-bit input? Write the structural VHDL program for the above design? 5M

4b) Design the logic circuit and write a structural-flow style VHDL program for the following function? $F(Q)=\sum_{A,B,C,B}(0,2,5,7,8,10,13,15) + D(11)$?

OR

5a) Design the logic circuit and write the data-flow style VDHL program for the following functions a)$F(X)= \sum_{A,B,C,D}(0,2,5,7,8,10,13,15) + D(1,6,11)$ 3M

b) $F(Y)= \sum_{A,B,C,D}(1,4,5,7,9,11,12,13,1,5)$ 3M

5b) what is the importance of time dimension in VHDL and explain its function? 4M

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-1** **Sign of the Invigilator**
	MID – I OBJECTIVE PAPER	**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

1. MOSFET is a [ ]

(a) Current controlled device (b) voltage controlled device (c) both (d) none

2. In MOSFET which region is used for amplification [ ]

(a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

3. CMOS Logic levels [ ]

(a) 0-2.0v & 4.0-5.0v (b) 0-1.5v & 3.5-5.0v (c) 0-2.3v & 3.7-5.0v (d) 0-1.9v & 3.1-5.0v

4. MOSFET is a [ ]

(a) Square law device (b) exponential device (c) constant device (d) none of the above

5. Input impedance of MOSFET is [ ]

(a) Very high (b) high (c) very low (d) low

6. Which of the following statements is incorrect? [ ]

(a)ECL has high power consumption.(b) ECL is widely used in high-speed applications.

(c)ECL is one of the fastest forms of electronic logic.(d)ECL suffers from low noise immunity.

7. RCTL stands for_____

8. Fastest logic gate family is [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

9. Which of the following family not belongs to bipolar logic gate families [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

10. The logic gate which has highest fan-out is [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-1** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

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(a) Current controlled device (b) voltage controlled device (c) both (d) none

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(a)RTL (b)DTL (c)ECL (d)CMOS

11. VHISC is an acronym for _____

12. The HDL compiler analyzes our code for [ ]

(a)Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

13. A VHDL Entity gives [ ]

(a)External behavior or declaration of modules (b) Internal behavior or structure

(c)Both (d) None of the above

14. The process which used to verify that the circuit work as desired is called[ ]

(a)Testing (b) Compilation (c) Simulation (d) Synthesis

15. DTL stands for _____

16. The Structural style of model consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

17. The Behavioral style of modeling consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

18. “A component instantiated in structural description must first be declared using a Component declaration”. The statement is (TRUE/FALSE)

19. A Component declaration declares [ ]

(a) Name of the component (b) Interface of the component

(c) Both (a) and (b) (d) None of the above

20. The Dataflow modeling consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

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11. VHISC is an acronym for _____

12. The HDL compiler analyzes our code for [ ]

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(c) Component declaration (d) Component declaration & instantiation

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-2** **Sign of the Invigilator**
	MID – I OBJECTIVE PAPER	**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

1. CMOS logic circuit operates from a_____ power supply

2. In PMOS as Vgs (gate to source voltage) decreases Rds (drain to source resistance

(a) Increases (b) Decreases(c) Remains constant (d) none of the above [ ]

3. In NMOS as Vgs(gate to source voltage) increases Rds(drain to source resistance [ ]

(a) Increases (b) Decreases(c) Remains constant (d) none of the above

4. In CMOS as fan-in increases on resistance of the series transistors [ ]

(a) Increases (b) Decreases(c) Remains constant (d) none of the above

5. Which of the following topic not comes under static behavior of the CMOS [ ]

(a) Fan out (b) logic levels (c) noise margins (d) Transition time

6. HTL is a modified form of [ ]

(a) DCTL (b) DTL (c) TTL (d) ECL

7. Fastest logic gate family is [ ]

(a) RTL (b) DTL (c) ECL (d) CMOS

8. Bipolar junction transistor acts as a _____

9. The voltage levels of ECL gate [ ]

(a) -1.8v and 0.8 (b) -0.8 and 1.8 (c) -2.3v and 3.7 (d) -1.9v and 3.1

10. In Bipolar Junction Transistors which region is used for amplification [ ]

(a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-2** **Sign of the Invigilator**
	MID – I OBJECTIVE PAPER	**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

1. CMOS logic circuit operates from a_____ power supply
2. In PMOS as Vgs (gate to source voltage) decreases Rds (drain to source resistance
   (a) Increases (b) Decreases(c) Remains constant (d) none of the above [ ]
3. In NMOS as Vgs(gate to source voltage) increases Rds(drain to source resistance [ ]
   (a) Increases (b) Decreases(c) Remains constant (d) none of the above
4. In CMOS as fan-in increases on resistance of the series transistors [ ]
   (a) Increases (b) Decreases(c) Remains constant (d) none of the above
5. Which of the following topic not comes under static behavior of the CMOS [ ]
   (a) Fan out (b) logic levels (c) noise margins (d) Transition time
6. HTL is a modified form of [ ]
   (a) DCTL (b) DTL (c) TTL (d) ECL
7. Fastest logic gate family is [ ]
   (a) RTL (b) DTL (c) ECL (d) CMOS
8. Bipolar junction transistor acts as a _____
9. The voltage levels of ECL gate [ ]
   (a) -1.8v and 0.8 (b) -0.8 and 1.8 (c) -2.3v and 3.7 (d) -1.9v and 3.1
10. In Bipolar Junction Transistors which region is used for amplification [ ]
    (a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

11. The HDL compiler analyzes our code for [ ]

(a) Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

12. A VHDL Architecture gives [ ]

(a)External behavior or declaration of modules (b) internal behavior or structure

(c) Both (d) None of the above

13. The buffer mode specifies [ ]

(a) Input of the entity (b)Output of the entity

(c)Either input or output (d)None of the above

14. The in out mode specifies [ ]

(a) Input of the entity (b) Output of the entity

(c) Either input or output (d)None of the above

15. In type STD-ULOGIC 'U' stands for _____

16. The Interface of the component specifies [ ]

(a) Mode of the port (b) Type of the port (c) Both (a) and (b) (d) None of the above

17. "In concurrent statements the ordering is most important".

The statement is

(TRUE/FALSE)

18. Which of the following statement come under behavioral modeling [ ]

(a) Wait Statement (b) If Statement (c) Case Statement (d) All the above

19. The Dataflow modeling consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

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	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-3** **Sign of the Invigilator**
	MID – I OBJECTIVE PAPER	**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** / **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

1. Which of the following topic not comes under static behavior of the CMOS? [ ]

   (a) Fan out (b) logic levels (c) noise margins (d) Transition time

2. The ability of an output to charge and discharge the stray capacitance is sometimes called _____

3. Compare to other logic families CMOS fan-out is [ ]

   (a) More (b) less (c) equal (d) less than or equal

4 .CMOS logic gates has [ ]

(a) less power consumption (b) high fan-out (c) low noise margin (d) both (a) and (b)

5. The amount of time that the output of logic circuit takes to change from one state to another is called the_____

6. HTL is a modified form of [ ]

   (a) DCTL (b) DTL (c) TTL (d)ECL

   10. DCTL stands for _____

7. Which of the following family not belongs to bipolar logic gate families [ ]

   (a)RTL (b)DTL (c)ECL (d)CMOS

8. Fastest logic gate family is [ ]

   (a)RTL (b)DTL (c)ECL (d)CMOS

9. The logic gate which has highest fan-out is [ ]

   (a)RTL (b)DTL (c)ECL (d)CMOS

10. When the current flows into TTL output in LOW state, the output is said to be _____

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-3** **Sign of the Invigilator**

	MID – I OBJECTIVE PAPER		**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM**	**ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**		**Max. Marks: 10M**
		Regd.No.	

1. Which of the following topic not comes under static behavior of the CMOS? [ ]

   (a) Fan out (b) logic levels (c) noise margins (d) Transition time

2. The ability of an output to charge and discharge the stray capacitance is sometimes called _____

3. Compare to other logic families CMOS fan-out is [ ]

   (a) More (b) less (c) equal (d) less than or equal

4 .CMOS logic gates has [ ]

(a) less power consumption (b) high fan-out (c) low noise margin (d) both (a) and (b)

5. The amount of time that the output of logic circuit takes to change from one state to another is called the_____

6. HTL is a modified form of [ ]

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   (a)RTL (b)DTL (c)ECL (d)CMOS

10. When the current flows into TTL output in LOW state, the output is said to be _____

11. The signals which are defined within the Package are [ ]

(a) global signals (b) local signals (c) Both (d)none

12.The VHDL Compiler automatically creates and uses a library named [ ]

(a) User defined library (b) Work library (c) STD-ULOGIC (d) Enumerated type

13. In type STD-ULOGIC 'X' stands for _____

14. The HDL compiler analyzes our code for [ ]

(a) Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

15. The buffer mode specifies [ ]

(a) Input of the entity (b) Output of the entity

(c) Either input or output (d) none of the above

16. The Interface of the component specifies [ ]

(a) Mode of the port (b) Type of the port (c) Both (a) and (b) (d) None of the above

17. "In concurrent statements the ordering is most important".

The statement is

(TRUE/FALSE)

18. Which of the following statement come under behavioral modeling [ ]

(a) Wait Statement (b) If Statement (c) Case Statement (d) All the above

19. The Dataflow modeling consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

20. A Component declaration declares [ ]

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	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-4** **Sign of the Invigilator**
	MID – I OBJECTIVE PAPER	**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** / **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

1. Which of the following is sequential statement [ ]

(a) NULL (b) LOOP (c) EXIT (d) All the above

2. The VHDL Simulator is used to [ ]

(a) To correct syntax errors (b) To identify semantic errors

(c) To observe the operation (d) To identify syntax errors

3. Which of the following statements not come under Dataflow modeling [ ]

(a) Case Statement (b) Block statements

(c) Concurrent assertion statements (d) Selected signal assignment statements

4. A Component declaration declares [ ]

(a) Name of the component (b) Interface of the component

(c) Both (a) and (b) (d) None of the above

5. The Structural style of model consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

6. HTL is a modified form of [ ]

(a) DCTL (b) DTL (c) TTL (d) ECL

7. Fastest logic gate family is [ ]

(a) RTL (b) DTL (c) ECL (d) CMOS

8. Bipolar junction transistor acts as a _____

9. The voltage levels of ECL gate [ ]

(a) -1.8v and 0.8 (b) -0.8 and 1.8 (c) -2.3v and 3.7 (d) -1.9v and 3.1

10. In Bipolar Junction Transistors which region is used for amplification [ ]

(a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-4** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 09-09.2019**
Year & Semester:	**III B.Tech, I SEM** **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN(15A04504)**	**Max. Marks: 10M**
	Regd.No.	

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2. The VHDL Simulator is used to [ ]

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(c) To observe the operation (d) To identify syntax errors

3. Which of the following statements not come under Dataflow modeling [ ]

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(c) Concurrent assertion statements (d) Selected signal assignment statements

4. A Component declaration declares [ ]

(a) Name of the component (b) Interface of the component

(c) Both (a) and (b) (d) None of the above

5. The Structural style of model consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

6. HTL is a modified form of [ ]

(a) DCTL (b) DTL (c) TTL (d) ECL

7. Fastest logic gate family is [ ]

(a) RTL (b) DTL (c) ECL (d) CMOS

8. Bipolar junction transistor acts as a _____

9. The voltage levels of ECL gate [ ]

(a) -1.8v and 0.8 (b) -0.8 and 1.8 (c) -2.3v and 3.7 (d) -1.9v and 3.1

10. In Bipolar Junction Transistors which region is used for amplification [ ]

(a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

11. VHISC is an acronym for _____

12. The HDL compiler analyzes our code for [ ]

(a)Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

13. A VHDL Entity gives [ ]

(a)External behavior or declaration of modules (b) Internal behavior or structure

(c)Both (d) None of the above

14. The process which used to verify that the circuit work as desired is called [ ]

(a)Testing (b) Compilation (c) Simulation (d) Synthesis

15. DTL stands for _____

16. The Interface of the component specifies [ ]

(a) Mode of the port (b) Type of the port (c) Both (a) and (b) (d) None of the above

17. "In concurrent statements the ordering is most important". The statement is (TRUE/FALSE)

18. Which of the following statement come under behavioral modeling [ ]

(a) Wait Statement (b) If Statement (c) Case Statement (d) All the above

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11. VHISC is an acronym for _____

12. The HDL compiler analyzes our code for [ ]

(a)Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

13. A VHDL Entity gives [ ]

(a)External behavior or declaration of modules (b) Internal behavior or structure

(c)Both (d) None of the above

14. The process which used to verify that the circuit work as desired is called [ ]

(a)Testing (b) Compilation (c) Simulation (d) Synthesis

15. DTL stands for _____

16. The Interface of the component specifies [ ]

(a) Mode of the port (b) Type of the port (c) Both (a) and (b) (d) None of the above

17. "In concurrent statements the ordering is most important". The statement is (TRUE/FALSE)

18. Which of the following statement come under behavioral modeling [ ]

(a) Wait Statement (b) If Statement (c) Case Statement (d) All the above

19. The Dataflow modeling consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

20. A Component declaration declares [ ]

(a) Name of the component (b) Interface of the component

(c) Both (a) and (b) (d) None of the above

Code: 15A04504 SET 1 R15

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

Department of ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech III Year I Sem (R15) First Mid-term Examinations, 09 September, 2019

DIGITAL SYSTEM DESIGN

Time: 90 minutes Max.Marks:30

Part – A

(Compulsory Question)

Answer the following: (5 x 2 = 10 Marks)

1. Explain about the CMOS Logic MOS Transistors?
2. Difference between Schottky transistor and Standard TTL?
3. Briefly describe the program structure of VHDL?
4. What are the various types of objects in VHDL and give the necessary examples?
5. How schottky transistors are formed and state its use?

Part-B

Note: Answer **TWO** Questions; Either 2nd Question or 3rd Question & Either 4th Question or 5th question

2a) Explain how CMOS_TTL interfacing can be achieved. Give the input and output levels of voltages and explain the same? 5M

2b) Explain about basic CMOS Inverter Circuit with functional behavior and switch model operation? 5M

OR

3a) Design a 4-input CMOS AND-OR-INVERT gate? Explain the circuit with the help of logic diagram and function table? 4M

3 b) Draw the circuit diagram of two input 10K ECL OR/NOR gate and explain its operation? 6M

4a) Discuss the steps in VHDL design flow. 6M

4b) Explain the difference in program of VHDL and any other procedural language. Give example? 4M

OR

5a) Design the logic circuit and write the data-flow style VDHL program for the following functions F(Y)= $\sum_{A,B,C,D}(1,4,5,7,9,11,12,13,1,5)$ 6M

5b) Design the logic circuit and write a structural-flow style VHDL program for the following function? F(Q)=$\prod_{P,R,R,S}(1,3,4,5,6,7,9,12,13,14)$? 4M

Code: 15A04504 SET 2 R15

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

Department of ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech III Year I Sem (R15) First Mid-term Examinations, 09 September, 2019

DIGITAL SYSTEM DESIGN

Time: 90 minutes Max.Marks:30

Part – A

(Compulsory Question)

Answer the following: (5 x 2 = 10 Marks)

1. Explain how a CMOS device is destroyed?
2. Explain about positive ECL (PECL)?
3. What are the constants of objects in VHDL and write the syntax with necessary examples?
4. Explain about the functions of VHDL with syntax and example
5. Mention the important characteristics of digital IC's?

Part-B

Note: Answer **TWO** Questions; Either 2nd Question or 3rd Question & Either 4th Question or 5th question

2a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation? 6M

2b) What is interfacing? Explain interfacing between low voltage CMOS logic, can it tolerate input voltage greater than $v_{cc,}$ if not explain? 4M

OR

3a) Explain how CMOS_TTL interfacing can be achieved. Give the input and output levels of voltages and explain the same? 4M

3b) Draw the circuit diagram of two inputs LS_ TTL NOR gate and explain the functional behavior? 6M

4a) Explain structural design elements of VHDL with example? 6M

4b) Write a behavioral style VHDL program for the following functions 4M

a) $F(S)=A+B+C^1$
b) $F(C_0)= AB+AC^1+BC^1$

OR

5a) Design the logic circuit and write a data-flow style VHDL program for the following function? $F(X)= \sum_{A,B,C,D}(1,5,6,7,9,13) + D(4,15)$ 4M+6M

5b) what are the various types of objects in VHDL and give the necessary examples?

Code: 15A04504 SET 3 R15

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

Department of ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech III Year I Sem (R15) First Mid-term Examinations, 09 September, 2019

DIGITAL SYSTEM DESIGN

Time: 90 minutes Max.Marks:30

Part – A

(Compulsory Question)

Answer the following: (5 x 2 = 10 Marks)

1. Explain about CMOS Logic. Sketch 2-input CMOS NAND gate .Explain their operation?
2. Explain the following terms with reference to CMOS logic? i. Logic Levels ii. DC Noise margin with typical i/p & o/p transfer characteristics of a CMOS Inverter
3. What is pure function and impure function? Explain with example?
4. Explain about the procedures in VHDL and write its syntax?
5. Write the comparison between TTL, CMOS, and ECL

Part-B

Note: Answer **TWO** Questions; Either 2nd Question or 3rd Question & Either 4th Question or 5th question

2a) Explain how CMOS_TTL interfacing can be achieved. Give the input and output levels of voltages and explain the same? 6M

2b) Draw the circuit diagram of two inputs LS_ TTL NOR gate and explain the functional behavior? 4M

OR

3a) Draw the resistive model of a CMOS inverter circuit and explain circuit behavior with resistive loads for LOW and HIGH outputs? 4M

3b) What is interfacing? Explain interfacing between low voltage CMOS logic, can it tolerate input voltage greater than $v_{cc,}$ if not explain? 6M

4a) Explain Behavioral design elements of VHDL? 4M

4b) Design a logic circuit to detect prime number of a 4-bit input? Write the structural VHDL program for the above design? 6M

OR

5a) Explain the use of packages. Give syntax and structure of a package in VHDL

5b)Design the logic circuit and write a data-flow style VHDL program for the following function? F(X)= $\sum_{A,B,C,D}(1,5,6,7,9,13) + D(4,15)$ 5M+5M

Code: 15A04504 SET 4 R15

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

Department of ELECTRONICS & COMMUNICATION ENGINEERING

B.Tech III Year I Sem (R15) First Mid-term Examinations, 09 September, 2019

DIGITAL SYSTEM DESIGN

Time: 90 minutes Max.Marks:30

Part – A

(Compulsory Question)

Answer the following: (5 x 2 = 10 Marks)

1. Explain about the following factors consider in TTL/CMOS interfacing
   a) Noise margin b)Fan out c) capacitive load
2. Explain about positive ECL (PECL)?
3. Explain how a CMOS device is destroyed?
4. Draw the two input ECL OR/NOR Gate and explain the operation with functional table and truth table?
5. What is High Threshold Logic?

Part-B

Note: Answer **TWO** Questions; Either 2nd Question or 3rd Question & Either 4th Question or 5th question

2a) Explain about basic CMOS Inverter Circuit with functional behavior and switch model operation? 5M

2b) Compare HC, HCT, VHC and VHCT CMOS logic families with the help of output specifications with VCC from 4.5V to 5.5V? 5M

OR

3a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation 5M

3b) What is interfacing? Explain interfacing between low voltage CMOS logic, can it tolerate input voltage greater than vcc, if not explain? 5M

4a) Design a logic circuit to detect prime number of a 5-bit input? Write the structural VHDL program for the above design? 5M

4b) Design the logic circuit and write a structural-flow style VHDL program for the following function? $F(Q)=\sum_{A,B,C,B}(0,2,5,7,8,10,13,15) + D(11)$?

OR

5a) Design the logic circuit and write the data-flow style VDHL program for the following functions a)$F(X)= \sum_{A,B,C,D}(0,2,5,7,8,10,13,15) + D(1,6,11)$ 3M

b) $F(Y)= \sum_{A,B,C,D}(1,4,5,7,9,11,12,13,1,5)$ 3M

5b) what is the importance of time dimension in VHDL and explain its function? 4M

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-1** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 08.01.2021**
Year & Semester:	**III B.Tech, I SEM** **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN**	**Max. Marks: 10M**
	Regd.No.	

1. MOSFET is a [ ]

(a) Current controlled device (b) voltage controlled device (c) both (d) none

2. In MOSFET which region is used for amplification [ ]

(a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

3. CMOS Logic levels [ ]

(a) 0-2.0v & 4.0-5.0v (b) 0-1.5v & 3.5-5.0v (c) 0-2.3v & 3.7-5.0v (d) 0-1.9v & 3.1-5.0v

4. MOSFET is a [ ]

(a) Square law device (b) exponential device (c) constant device (d) none of the above

5. Input impedance of MOSFET is [ ]

(a) Very high (b) high (c) very low (d) low

6. Which of the following statements is incorrect? [ ]

(a)ECL has high power consumption.(b) ECL is widely used in high-speed applications.

(c)ECL is one of the fastest forms of electronic logic.(d)ECL suffers from low noise immunity.

7. RCTL stands for_____

8. Fastest logic gate family is [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

9. Which of the following family not belongs to bipolar logic gate families [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

10. The logic gate which has highest fan-out is [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-1** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 08.01.2021**
Year & Semester:	**III B.Tech, I SEM** **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN**	**Max. Marks: 10M**
	Regd.No.	

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2. In MOSFET which region is used for amplification [ ]

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11. VHISC is an acronym for _____

12. The HDL compiler analyzes our code for [ ]

(a)Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

13. A VHDL Entity gives [ ]

(a)External behavior or declaration of modules (b) Internal behavior or structure

(c)Both (d) None of the above

14. The process which used to verify that the circuit work as desired is called [ ]

(a)Testing (b) Compilation (c) Simulation (d) Synthesis

15. DTL stands for _____

16. The Structural style of model consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

17. The Behavioral style of modeling consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

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18. “A component instantiated in structural description must first be declared using a Component declaration”. The statement is (TRUE/FALSE)

19. A Component declaration declares [ ]

(a) Name of the component (b) Interface of the component

(c) Both (a) and (b) (d) None of the above

20. The Dataflow modeling consists of [ ]

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	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-2** **Sign of the Invigilator**
	MID – I OBJECTIVE PAPER	**DATE: 08.01.2021**
Year & Semester:	**III B.Tech, I SEM** | **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN**	**Max. Marks: 10M**
	Regd.No.	

1. CMOS logic circuit operates from a_____ power supply

2. In PMOS as Vgs (gate to source voltage) decreases Rds (drain to source resistance [ ]

(a) Increases (b) Decreases(c) Remains constant (d) none of the above

3. In NMOS as Vgs(gate to source voltage) increases Rds(drain to source resistance [ ]

(a) Increases (b) Decreases(c) Remains constant (d) none of the above

4. In CMOS as fan-in increases on resistance of the series transistors [ ]

(a) Increases (b) Decreases(c) Remains constant (d) none of the above

5. Which of the following topic not comes under static behavior of the CMOS [ ]

(a) Fan out (b) logic levels (c) noise margins (d) Transition time

6. HTL is a modified form of [ ]

(a) DCTL (b) DTL (c) TTL (d) ECL

7. Fastest logic gate family is [ ]

(a) RTL (b) DTL (c) ECL (d) CMOS

8. Bipolar junction transistor acts as a _____

9. The voltage levels of ECL gate [ ]

(a) -1.8v and 0.8 (b) -0.8 and 1.8 (c) -2.3v and 3.7 (d) -1.9v and 3.1

10. In Bipolar Junction Transistors which region is used for amplification [ ]

(a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-2** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 08.01.2021**
Year & Semester:	**III B.Tech, I SEM** | **Branch: ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN**	**Max. Marks: 10M**
	Regd.No.	

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(a) Increases (b) Decreases(c) Remains constant (d) none of the above

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11. The HDL compiler analyzes our code for [ ]

(a) Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

12. A VHDL Architecture gives [ ]

(a)External behavior or declaration of modules (b) internal behavior or structure

(c) Both (d) None of the above

13. The buffer mode specifies [ ]

(a) Input of the entity (b)Output of the entity

(c)Either input or output (d)None of the above

14. The in out mode specifies [ ]

(a) Input of the entity (b) Output of the entity

(c) Either input or output (d)None of the above

15. In type STD-ULOGIC 'U' stands for _____

16. The Interface of the component specifies [ ]

(a) Mode of the port (b) Type of the port (c) Both (a) and (b) (d) None of the above

17. "In concurrent statements the ordering is most important".

The statement is (TRUE/FALSE)

18. Which of the following statement come under behavioral modeling [ ]

(a) Wait Statement (b) If Statement (c) Case Statement (d) All the above

19. The Dataflow modeling consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

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	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-3** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 08.01.2021**
Year & Semester:	**III B.Tech, I SEM** **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN**	**Max. Marks: 10M**
	Regd.No.	

1. Which of the following topic not comes under static behavior of the CMOS? [ ]

(a) Fan out (b) logic levels (c) noise margins (d) Transition time

2. The ability of an output to charge and discharge the stray capacitance is sometimes called _____

3. Compare to other logic families CMOS fan-out is [ ]

(a) More (b) less (c) equal (d) less than or equal

4 .CMOS logic gates has [ ]

(a) less power consumption (b) high fan-out (c) low noise margin (d) both (a) and (b)

5. The amount of time that the output of logic circuit takes to change from one state to another is called the_____

6. HTL is a modified form of [ ]

(a) DCTL (b) DTL (c) TTL (d)ECL

10. DCTL stands for _____

7. Which of the following family not belongs to bipolar logic gate families [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

8. Fastest logic gate family is [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

9. The logic gate which has highest fan-out is [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

10. When the current flows into TTL output in LOW state, the output is said to be _____

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-3** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 08.01.2021**
Year & Semester:	**III B.Tech, I SEM** **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN**	**Max. Marks: 10M**
	Regd.No.	

1. Which of the following topic not comes under static behavior of the CMOS? [ ]

(a) Fan out (b) logic levels (c) noise margins (d) Transition time

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9. The logic gate which has highest fan-out is [ ]

(a)RTL (b)DTL (c)ECL (d)CMOS

10. When the current flows into TTL output in LOW state, the output is said to be _____

11. The signals which are defined within the Package are [ ]

(a) global signals (b) local signals (c) Both (d)none

12.The VHDL Compiler automatically creates and uses a library named [ ]

(a) User defined library (b) Work library (c) STD-ULOGIC (d) Enumerated type

13. In type STD-ULOGIC 'X' stands for _____

14. The HDL compiler analyzes our code for [ ]

(a) Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

15. The buffer mode specifies [ ]

(a) Input of the entity (b) Output of the entity

(c) Either input or output (d) none of the above

16. The Interface of the component specifies [ ]

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17. "In concurrent statements the ordering is most important".

The statement is (TRUE/FALSE)

18. Which of the following statement come under behavioral modeling [ ]

(a) Wait Statement (b) If Statement (c) Case Statement (d) All the above

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(c) Both (a) and (b) (d) None of the above

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-4** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 08.01.2021**
Year & Semester:	**III B.Tech, I SEM** / **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN**	**Max. Marks: 10M**
	Regd.No.	

1. Which of the following is sequential statement [ ]

(a) NULL (b) LOOP (c) EXIT (d) All the above

2. The VHDL Simulator is used to [ ]

(a) To correct syntax errors (b) To identify semantic errors

(c) To observe the operation (d) To identify syntax errors

3. Which of the following statements not come under Dataflow modeling [ ]

(a) Case Statement (b) Block statements

(c) Concurrent assertion statements (d) Selected signal assignment statements

4. A Component declaration declares [ ]

(a) Name of the component (b) Interface of the component

(c) Both (a) and (b) (d) None of the above

5. The Structural style of model consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

6. HTL is a modified form of [ ]

(a) DCTL (b) DTL (c) TTL (d) ECL

7. Fastest logic gate family is [ ]

(a) RTL (b) DTL (c) ECL (d) CMOS

8. Bipolar junction transistor acts as a _____

9. The voltage levels of ECL gate [ ]

(a) -1.8v and 0.8 (b) -0.8 and 1.8 (c) -2.3v and 3.7 (d) -1.9v and 3.1

10. In Bipolar Junction Transistors which region is used for amplification [ ]

(a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

	RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN **Nandikotkur Road, Kurnool – 518 004**	**SET-4** **Sign of the Invigilator**
MID – I OBJECTIVE PAPER		**DATE: 08.01.2021**
Year & Semester:	**III B.Tech, I SEM** / **ECE**	**TIME: 20 MIN**
Name of the Subject:	**DIGITAL SYSTEM DESIGN**	**Max. Marks: 10M**
	Regd.No.	

1. Which of the following is sequential statement [ ]

(a) NULL (b) LOOP (c) EXIT (d) All the above

2. The VHDL Simulator is used to [ ]

(a) To correct syntax errors (b) To identify semantic errors

(c) To observe the operation (d) To identify syntax errors

3. Which of the following statements not come under Dataflow modeling [ ]

(a) Case Statement (b) Block statements

(c) Concurrent assertion statements (d) Selected signal assignment statements

4. A Component declaration declares [ ]

(a) Name of the component (b) Interface of the component

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8. Bipolar junction transistor acts as a _____

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10. In Bipolar Junction Transistors which region is used for amplification [ ]

(a) Active region (b) Cutoff region (c) Saturation region (d) both active and cutoff

11. VHISC is an acronym for _____

12. The HDL compiler analyzes our code for [ ]

(a)Technical errors (b) Syntax errors (c) Compatibility (d) Both (b) and (c)

13. A VHDL Entity gives [ ]

(a)External behavior or declaration of modules (b) Internal behavior or structure

(c)Both (d) None of the above

14. The process which used to verify that the circuit work as desired is called [ ]

(a)Testing (b) Compilation (c) Simulation (d) Synthesis

15. DTL stands for _____

16. The Interface of the component specifies [ ]

(a) Mode of the port (b) Type of the port (c) Both (a) and (b) (d) None of the above

17. "In concurrent statements the ordering is most important". The statement is (TRUE/FALSE)

18. Which of the following statement come under behavioral modeling [ ]

(a) Wait Statement (b) If Statement (c) Case Statement (d) All the above

19. The Dataflow modeling consists of [ ]

(a) Sequential Statements (b) Concurrent Statements

(c) Component declaration (d) Component declaration & instantiation

20. A Component declaration declares [ ]

(a) Name of the component (b) Interface of the component

(c) Both (a) and (b) (d) None of the above

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13. A VHDL Entity gives [ ]

(a)External behavior or declaration of modules (b) Internal behavior or structure

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16. The Interface of the component specifies [ ]

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18. Which of the following statement come under behavioral modeling [ ]

(a) Wait Statement (b) If Statement (c) Case Statement (d) All the above

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20. A Component declaration declares [ ]

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RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL
B.Tech – III-I Semester (R15) MID I Examinations
Branch: ECE

SET-1

Sub: DSD **Date: 08-01-2020**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Which is faster TTL or ECL? Which requires more power to operate?	**2**	**1**	C303.2	Understand
ii)	State the characteristics of CMOS family.	**2**	**1**	C303.1	Analyze
iii)	Write the HDL data flow description of 4 bit adder.	**2**	**2**	C303.3	Remember
iv)	Sketch the VHDL program file structure.	**2**	**2**	C303.3	Remember
v)	Write the syntax for VHDL function declaration.	**2**	**1**	C303.1	Remember
2. a)	Design logic diagram for AND-OR-INVERT gate. Construct the same using CMOS logic and analyze the circuit with the help of function table.	**6**	**1**	C303.1	Understand
b)	Design and summarize the internal 3 sections of LS-TTL NAND gate and analyze the circuit with the help of function table.	**4**	**1**	C303.1	Understand
3.a)	With suitable diagrams, explain the interfacing of low voltage CMOS logic with TTL logic family.	**6**	**1**	C303.2	Understand
b)	Design a CMOS inverter and explain its operation. Comment on its characteristics such as FAN-in, Fan-out, power dissipation, and propagation delay and noise margin. Compare its advantages over other logic families.	**4**	**1**	C303.2	Evaluate
4.a)	Model the design flow of VHDL program with front-end and back-end steps.	**5**	**2**	C303.3	Understand
b)	Develop a structural VHDL program for a 4-bit prime number detector.	**5**	**2**	C303.3	Understand
5.a)	Enumerate on the structural design elements and behavioural design elements of VHDL with suitable examples.	**6**	**2**	C303.3	Understand
b)	Outline the function of test benches of VHDL.	**4**	**2**	C303.3	Remember

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL
B.Tech – III-I Semester (R15) MID I Examinations
Branch: ECE

SET-1

Sub: DSD **Date: 08-01-2020**
Time: 1½ Hrs. **Max Marks: 30M**

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v)	Write the syntax for VHDL function declaration.	**2**	**1**	C303.1	Remember
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b)	Design and summarize the internal 3 sections of LS-TTL NAND gate and analyze the circuit with the help of function table.	**4**	**1**	C303.1	Understand
3.a)	With suitable diagrams, explain the interfacing of low voltage CMOS logic with TTL logic family.	**6**	**1**	C303.2	Understand
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b)	Develop a structural VHDL program for a 4-bit prime number detector.	**5**	**2**	C303.3	Understand
5.a)	Enumerate on the structural design elements and behavioural design elements of VHDL with suitable examples.	**6**	**2**	C303.3	Understand
b)	Outline the function of test benches of VHDL.	**4**	**2**	C303.3	Remember

SET-2

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL
B.Tech – III-I Semester (R15) MID I Examinations
Branch: ECE

Sub: DSD **Date: 08-01-2020**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Define propagation delay.	2	1	C303.1	Remember
ii)	Which logic family has highest speed of operation?	2	1	C303.1	Understand
iii)	What is architecture in VHDL?	2	2	C303.3	Understand
iv)	What are the data types in VHDL?	2	2	C303.3	Remember
v)	Classify the logic family by operation.	2	3	C303.2	Remember
2. a)	With a neat circuit diagram, explain the operation of a TTL open collector output.	5	1	C303.2	Remember
b)	With a neat circuit diagram, explain the operation of a CMOS open drain and tristate outputs.	5	1	C303.1	Remember
3.a)	Explain in detail about comparison of different logic families.	5	2	C303.3	Understand
b)	Explain IC interfacing for TTL driving CMOS.	5	2	C303.3	Understand
4.a)	Explain different delays in VHDL.	6	2	C303.3	Understand
b)	Draw the design flow of VHDL and explain each block.	4	2	C303.3	Remember
5.a)	What are the types of objects in VHDL? Explain each block.	5	2	C303.3	Understand
b)	Explain concept of libraries in VHDL.	5	2	C303.3	Understand

SET-2

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL
B.Tech – III-I Semester (R15) MID I Examinations
Branch: ECE

Sub: DSD **Date: 08-01-2020**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Define propagation delay.	**2**	**1**	C303.1	Remember
ii)	Which logic family has highest speed of operation?	**2**	**1**	C303.1	Understand
iii)	What is architecture in VHDL?	**2**	**2**	C303.3	Understand
iv)	What are the data types in VHDL?	**2**	**2**	C303.3	Remember
v)	Classify the logic family by operation.	**2**	**3**	C303.2	Remember
2. a)	With a neat circuit diagram, explain the operation of a TTL open collector output.	**5**	**1**	C303.2	Remember
b)	With a neat circuit diagram, explain the operation of a CMOS open drain and tristate outputs.	**5**	**1**	C303.1	Remember
3.a)	Explain in detail about comparison of different logic families.	**5**	**2**	C303.3	Understand
b)	Explain IC interfacing for TTL driving CMOS.	**5**	**2**	C303.3	Understand
4.a)	Explain different delays in VHDL.	**6**	**2**	C303.3	Understand
b)	Draw the design flow of VHDL and explain each block.	**4**	**2**	C303.3	Remember
5.a)	What are the types of objects in VHDL? Explain each block.	**5**	**2**	C303.3	Understand
b)	Explain concept of libraries in VHDL.	**5**	**2**	C303.3	Understand

SET-3

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL
B.Tech – III-I Semester (R15) MID I Examinations
Branch: ECE

Sub: DSD **Date: 08-01-2020**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Differentiate between the TTL and DTL logic families.	2	1	C303.2	Analyze
ii)	Give the characteristics of TTL logic family.	2	1	C303.2	Remember
iii)	What is logic synthesis?	2	2	C303.3	Remember
iv)	What are the behavioural design elements?	2	2	C303.3	Remember
v)	State the characteristics of CMOS family.	2	2	C303.3	Remember
2.a)	List out the advantages and disadvantages of ECL, TTL and CMOS logic family.	5	2	C303.3	understand
b)	Design a 2-input LS-TTL NAND gate and explain its operation. Give the function truth table.	5	2	C303.3	Create
3.a)	Design and explain the 2-input OR/NOR gate using ECL logic.	5	2	C303.3	Analyze
b)	List out the specifications of standards of 74XX and CMOS 40XX series ICs.	5	1	C303.2	Evaluate
4.a)	Explain about the different data types in Verilog HDL.	5	1	C303.2	understand
b)	Define simulation? Explain about gate-level simulation, behavioral simulation and functional simulation.	5	1	C303.2	understand
5.a)	Explain the packages and libraries of VHDL.	5	2	C303.3	Create
b)	Explain in detail about post layout timing simulation	5	2	C303.3	Analyze

SET-3

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL
B.Tech – III-I Semester (R15) MID I Examinations
Branch: ECE

Sub: DSD **Date: 08-01-2020**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Differentiate between the TTL and DTL logic families.	2	1	C303.2	Analyze
ii)	Give the characteristics of TTL logic family.	2	1	C303.2	Remember
iii)	What is logic synthesis?	2	2	C303.3	Remember
iv)	What are the behavioural design elements?	2	2	C303.3	Remember
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2.a)	List out the advantages and disadvantages of ECL, TTL and CMOS logic family.	5	2	C303.3	understand
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5.a)	Explain the packages and libraries of VHDL.	5	2	C303.3	Create
b)	Explain in detail about post layout timing simulation	5	2	C303.3	Analyze

SET-4

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL
B.Tech – III-I Semester (R15) MID I Examinations
Branch: ECE

Sub: DSD **Date: 08-01-2020**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Describe the key benefit of Schottky transistors in TTL.	**2**	**1**	C303.1	Remember
ii)	What are the disadvantages of ECL gates?	**2**	**2**	C303.3	Remember
iii)	Write the syntax for package.	**2**	**1**	C303.1	Remember
iv)	Discuss about technology libraries.	**2**	**1**	C303.2	Remember
v)	Which logic family has highest speed of operation?	**2**	**2**	C303.3	Remember
2. a)	How to interface CMOS with TTL logic. Give its constraints.	**5**	**1**	C303.1	understand
b)	Draw the circuit diagram of basic TTL NAND gate and explain with the help of functional operation.	**5**	**1**	C303.2	understand
3.a)	What are the salient features of ECL? And explain its internal structure.	**5**	**1**	C303.1	understand
b)	Compare various types of logic families.	**5**	**1**	C303.1	understand
4.(a)	Explain about the following: (i) Concurrency. (ii) Simulation. (iii) Synthesis. (iv) System tasks.	**5**	**2**	C303.3	understand
(b)	Explain about the data types, scalar and vector parameters, keywords in VHDL.	**5**	**2**	C303.3	Create
5.	Explain various primitives available in VHDL and give one example for one of the primitive.	**5**	**2**	C303.3	Evaluate
b.)	Explain about compiler directives.	**5**	**2**	C303.3	Create

SET-4

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN (3T), KURNOOL
B.Tech – III-I Semester (R15) MID I Examinations
Branch: ECE

Sub: DSD **Date: 08-01-2020**
Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

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1. i)	Describe the key benefit of Schottky transistors in TTL.	**2**	**1**	C303.1	Remember
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iii)	Write the syntax for package.	**2**	**1**	C303.1	Remember
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b.)	Explain about compiler directives.	**5**	**2**	C303.3	Create

SET1

Sign of Invigilator:

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL
III-YEAR I-SEM SECOND MID EXAMINATIONS – 05.03.2021
DIGITAL SYSTEM DESIGN
(Objective Type Test)

Date: 16 .11.2018 Max. Marks: 10

TIME: 20MIN BRANCH: ECE

1. One of the following is dual 2 to 4 decoder { }

a. 74LS139 b. 74X130 c. 74X129 d. 74X119

2. 10011 input in seven segments decodes as _ _ _ _ _ _ _ _ _ output. { }

a. 1111101 b. 1011001 c. 1111001 d. 1111000

3. _ _ _ _ _ _ _ _ is seven segment decoder { }

a. 74X138 b. 74X49 c. 74X491 d. 74X149

4. 10111 input gives _ _ _ _ _ _ _ _ _ _ _ _ output in seven segment decoder { }

a. 1110000 b. 1110001 c. 1110010 d. 1100000

5. 001111111 input produce _ _ _ _ _ _ _ _ in 74 X 148, 8 bit priority encoder. { }

a. 11001 b. 11101 c. 10101 d. 11100

6. 74x682 does not provide { }

a. greater than output b. less than output

c. equal output d. output

7. if then else VHDL statement used within { }

a. WHILE b. select c. process d. assert

8. For more flexible comparisions & arithmetic operations IEEE 1076-3 created a package. it is { }

a. std logic arith b. std logic ulogic

c. std logic 1164 d. std logic unsigned

9. In 74 x 181, if S3 S2 S1 S0 = 1100, M = 1, then F is { }

a. 1001 b. 1010 c. 1111 d. 0000

10. _ _ _ _ _ _ _ _ specify the direction of shift, type of shift and amount of shift. { }

a. Barrel shifter b. Carry save shifter

c. sequential shifter d. group ripple shifter

SET1

Sign of Invigilator:

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

III-YEAR I-SEM SECOND MID EXAMINATIONS –05.03.2021

DIGITAL SYSTEM DESIGN

(Objective Type Test)

Date: 16 .11.2018 Max. Marks: 10

TIME: 20MIN BRANCH: ECE

1. One of the following is dual 2 to 4 decoder { }

a. 74LS139 b. 74X130 c. 74X129 d. 74X119

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5. 001111111 input produce _ _ _ _ _ _ _ _ in 74 X 148, 8 bit priority encoder. { }

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10. _ _ _ _ _ _ _ _ specify the direction of shift, type of shift and amount of shift. { }

a. Barrel shifter b. Carry save shifter

c. sequential shifter d. group ripple shifter

11. . _ _ _ _ _ _ _ _ _ _ is the minimum delay between negative S & R(in S - R latch) for them to be considered no simultaneous. { }

a. Recovery time b. propagation time
c. delay time d. access time

12. _ _ _ _ _ _ _ _ _ _ is positive edge triggering D FlipFlop. { }

a. 74LS109 b. 74LS79 c. 74LS74 d. 74LS70

13. VHDL statement for positive edge triggered D FF is { }

a. Q < = D when clk' event and clk =`1' else Q;
b. Q < = D when clk' event and clk = `0' else not Q ;
c. Q < = not D when clk' event and clk = `1' else Q;
d. Q > = D when clk' event and clk =`0' else not Q;

14. _ _ _ _ _ _ _ _ contain four D latches. { }

a. 74 X 175 b. 74 X 74 c. 74 X 112 d. 74 X 375

15. _ _ _ _ _ _ _ _ _ _ is JKFF with active low clock input. { }

a. 74 × 74 b. 74 × 112 c. 74 × 375 d. 74 × 175

15. _ _ _ _ _ _ _ _ is 8K X 8 SRAM. { }

a. GAL22V10 b. 2764 c. HM6264 d. 74HC04

16. EPROMs will have { }

a. floating gate MOS b. floating source MOS
c. floating drain MOS d. floating body MOS

17. _ _ _ _ _ _ _ _ _ _ is 8K X 8 EPROM. { }

a. 2764 b. HM6264 c. 74 X 74 d. 74 X 112

18. _ _ _ _ _ _ _ _ _ _ _ input must be asserted to enable outputs in EPROM. { }

a. CS b. CLR L c. WE L d. output enable(OE)

19. In SRAMs output buffer is automatically disabled whenever _ _ _ _ _ _ _ _ is asserted ,even if OE _ L is asserted. { }

a. WE L b. WE H c. CLR L d. CLR H

20. EEPROM (NMOS Technology) Read cycle is { }

a. 500 - 1500ns b. 250 -1 200ms c. 250 - 300ns d. 50 - 200 ns

11. . _ _ _ _ _ _ _ _ _ _ is the minimum delay between negative S & R(in S - R latch) for them to be considered no simultaneous. { }

a. Recovery time b. propagation time

c. delay time d. access time

12. _ _ _ _ _ _ _ _ _ _ is positive edge triggering D FlipFlop. { }

a. 74LS109 b. 74LS79 c. 74LS74 d. 74LS70

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b. Q < = D when clk' event and clk = `0' else not Q ;

c. Q < = not D when clk' event and clk = `1' else Q;

d. Q > = D when clk' event and clk =`0' else not Q;

14. _ _ _ _ _ _ _ _ contain four D latches. { }

a. 74 X 175 b. 74 X 74 c. 74 X 112 d. 74 X 375

15. _ _ _ _ _ _ _ _ _ _ is JKFF with active low clock input. { }

a. 74 × 74 b. 74 × 112 c. 74 × 375 d. 74 × 175

15. _ _ _ _ _ _ _ _ is 8K X 8 SRAM. { }

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20. EEPROM (NMOS Technology) Read cycle is { }

a. 500 - 1500ns b. 250 -1 200ms c. 250 - 300ns d. 50 - 200 ns

Sign of Invigilator:

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

III-YEAR I-SEM SECOND MID EXAMINATIONS – 05.03.2021 **SET2**

DIGITAL SYSTEM DESIGN

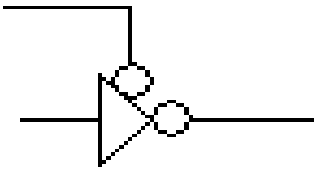
(Objective Type Test)

Date: 16 .11.2018 Max. Marks: 10

TIME: 20MIN BRANCH: ECE

1. The IDLE output in generic 8 input priority encoder is asserted if _ _ _ _ _ are asserted.
a. no inputs b. I1, I4 c. I2,I6 d. I4,I5 { }
2. _ _ _ _ _ _ _ must be asserted for any of its output to be asserted in 74 X 148 { }
a. EO _ H b. EO _ L c. EI _ L d. EI _ H
3. _ _ _ _ _ _ _ _ _ _ contains four independent Non - inverting three state buffer. { }
a. 74 X 120 b. 74 X 126 c. 74 X 129 d. 74 X 136
4. 0XX011111 gives _ _ _ _ _ _ _ _ output in priority encoder { }
a. 10100 b. 00101 c. 10001 d. 10101
5. _ _ _ _ _ _ _ _ is 8 bit comparator and has no cascading inputs. { }
a. 74 X 85 b. 74 X 138 c. 74 X 682 d. 74 X 153
6. _ _ _ _ _ _ _ _ _ _ _ _ is quadruple 2 input XOR gate. { }
a. 74 X 86 b. 74 X 280 c. 74 X 138 d. 74 X 153
7. _ _ _ _ _ _ _ _ _ is a 4 bit binary adder. { }
a.74 X 280 b. 74 X 283 c. 74 X 138 d. 74 X 153
8. _ _ _ _ _ _ _ provide group carry look ahead outputs. { }
a. 74 × 153 b. 74 × 280 c. 74 × 138 d. 74 × 381
9. A combinational fixed point to floating point encoder consists of { }
a. one 74 × 148, three 74 × 154
b. one 74 × 148, two 74 × 154, 74 × 251
c. two 74 × 154, 74 × 251
d. 74 × 280,two 74 × 138

10.Shown in figure (a) represents { }



Figure(a)

a. non Inverting active high enable buffer b. Inverting active high enable buffer

c. non Inverting active low enable buffer d. Inverting active low enable buffer

Sign of Invigilator:

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

III-YEAR I-SEM SECOND MID EXAMINATIONS – 05.03.2021

DIGITAL SYSTEM DESIGN **SET2**

(Objective Type Test)

Date: 16 .11.2018 Max. Marks: 10

TIME: 20MIN BRANCH: ECE

1. The IDLE output in generic 8 input priority encoder is asserted if _ _ _ _ _ are asserted.
a. no inputs b. I1, I4 c. I2,I6 d. I4,I5 { }

2. _ _ _ _ _ _ _ must be asserted for any of its output to be asserted in 74 X 148 { }
a. EO _ H b. EO _ L c. EI _ L d. EI _ H

3. _ _ _ _ _ _ _ _ _ _ contains four independent Non - inverting three state buffer. { }
a. 74 X 120 b. 74 X 126 c. 74 X 129 d. 74 X 136

4. 0XX011111 gives _ _ _ _ _ _ _ _ output in priority encoder { }
a. 10100 b. 00101 c. 10001 d. 10101

5. _ _ _ _ _ _ _ _ is 8 bit comparator and has no cascading inputs. { }
a. 74 X 85 b. 74 X 138 c. 74 X 682 d. 74 X 153

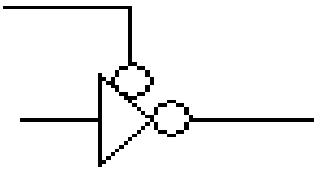
6. _ _ _ _ _ _ _ _ _ _ _ _ is quadruple 2 input XOR gate. { }
a. 74 X 86 b. 74 X 280 c. 74 X 138 d. 74 X 153

7. _ _ _ _ _ _ _ _ _ is a 4 bit binary adder. { }
a.74 X 280 b. 74 X 283 c. 74 X 138 d. 74 X 153

8. _ _ _ _ _ _ _ provide group carry look ahead outputs. { }
a. 74 × 153 b. 74 × 280 c. 74 × 138 d. 74 × 381

9. A combinational fixed point to floating point encoder consists of { }
a. one 74 × 148, three 74 × 154
b. one 74 × 148, two 74 × 154, 74 × 251
c. two 74 × 154, 74 × 251
d. 74 × 280,two 74 × 138

10.Shown in figure (a) represents { }



Figure(a)

a. non Inverting active high enable buffer b. Inverting active high enable buffer

c. non Inverting active low enable buffer d. Inverting active low enable buffer

11. _ _ _ _ _ _ _ _ _ _ is JKFF with active low clock input. { }
a. 74 × 74 b. 74 × 112 c. 74 × 375 d. 74 × 175
12. _ _ _ _ _ _ _ _ _ _ contains 4 bit register with a common clock and asynchronous clear input. { }
a. 74 × 375 b. 74 × 112 c. 74 × 370 d. 74 × 175
13. _ _ _ _ _ _ _ _ _ _ is 6 bit register. { }
a. 74 × 174 b. 74 × 375 c. 74 × 75 d. 74 × 112
14. _ _ _ _ _ _ _ _ _ _ is (octal edge trigger D FF) 8 bit register. { }
a. 74 × 174 b. 74 × 74 c. 74 × 374 d. 74 × 112
15. _ _ _ _ _ _ _ _ _ _ uses D latches. { }
a. 74 × 373 b. 74 × 174 c. 74 × 74 d. 74 × 112
16. For reliable synchronous design , one of the following is valid. { }
a. minimize amount of clock skew
b. synchronizers should have medium probability of failure
c. ensure FF have negative set up & hold time marging
d. maximize amount of clock skew

17. EPROM (CMOS Technology) Write cycle is { }

a. 50 - 100 µs /byte b. 10 - 50 µs/byte
c. 70 - 500 µs /byte d. 100 - 500 µs /byte
18. Two dimensional decoding allows a 128 X 1 ROM to be built with { }
a. 3 to 8 decoder and 16 input multiplexer
b. 2 to 4 decoder and 10 input multiplexer
c. 3 to 10 decoder and 20 input multiplexer
d. 10 to 1024 decoder and 1024 input multiplexer

19. A 1M X 1 ROM could be built with { }
a. 3 to 8 decoder and 16 input multiplexer
b. floating source MOS
c. 10 to 1024 decoder and 1024 input multiplexer
d. 3 to 10 decoder and 20 input multiplexer

20. _ _ _ _ _ _ _ _ _ _ is used to reduce the decoder size in ROM { }
a. one dimensional decoding
b. Two dimensional decoding
c. five dimensional decoding
d. four dimensional decoding

11. _ _ _ _ _ _ _ _ _ _ is JKFF with active low clock input. { }
a. 74 × 74 b. 74 × 112 c. 74 × 375 d. 74 × 175
12. _ _ _ _ _ _ _ _ _ _ contains 4 bit register with a common clock and asynchronous clear input. { }
a. 74 × 375 b. 74 × 112 c. 74 × 370 d. 74 × 175
13. _ _ _ _ _ _ _ _ _ _ is 6 bit register. { }
a. 74 × 174 b. 74 × 375 c. 74 × 75 d. 74 × 112
14. _ _ _ _ _ _ _ _ _ _ is (octal edge trigger D FF) 8 bit register. { }
a. 74 × 174 b. 74 × 74 c. 74 × 374 d. 74 × 112
15. _ _ _ _ _ _ _ _ _ _ uses D latches. { }
a. 74 × 373 b. 74 × 174 c. 74 × 74 d. 74 × 112
16. For reliable synchronous design , one of the following is valid. { }
a. minimize amount of clock skew
b. synchronizers should have medium probability of failure
c. ensure FF have negative set up & hold time marging
d. maximize amount of clock skew

17. EPROM (CMOS Technology) Write cycle is { }

a. 50 - 100 µs /byte b. 10 - 50 µs/byte
c. 70 - 500 µs /byte d. 100 - 500 µs /byte
18. Two dimensional decoding allows a 128 X 1 ROM to be built with { }
a. 3 to 8 decoder and 16 input multiplexer
b. 2 to 4 decoder and 10 input multiplexer
c. 3 to 10 decoder and 20 input multiplexer
d. 10 to 1024 decoder and 1024 input multiplexer

19. A 1M X 1 ROM could be built with { }
a. 3 to 8 decoder and 16 input multiplexer
b. floating source MOS
c. 10 to 1024 decoder and 1024 input multiplexer
d. 3 to 10 decoder and 20 input multiplexer

20. _ _ _ _ _ _ _ _ _ _ is used to reduce the decoder size in ROM { }
a. one dimensional decoding
b. Two dimensional decoding
c. five dimensional decoding
d. four dimensional decoding

Sign of Invigilator:

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL

III-YEAR I-SEM SECOND MID EXAMINATIONS – 05.03.2021

DIGITAL SYSTEM DESIGN **SET3**

(Objective Type Test)

Date: 16 .11.2018 Max. Marks: 10

TIME: 20MIN BRANCH: ECE

---

1. For 74 X 151, input 0001 produces { }

a. D1 & not D1 b. D1 & not D2 c. D5 & not D5 d. D5 & not D6

2. _ _ _ _ _ _ _ _ _ _ _ _ is 2 input, 4 bit multiplexer. { }

a. 74 X 541 b. 74 X 157 c. 74 X 155 d. 74 X 148

3. 32 input, 1 bit multiplexer contains

a. 74 X 139, four 74 X 151 b. 74 X 136, two 74 X 151

c. 74 X 131, four 74 X 155 d. 74 X 130, four 74 X 159

4. _ _ _ _ _ _ is 9 bit parity generator. { }

a. 74 X 153 b. 74 X 86 c. 74 X 138 d. 74 X 280

5. _ _ _ _ _ _ _ _ has cascading inputs for combining multiple '85s to create comparator for more than four bits. { }

a. 74 X 85 b. 74 X 280 c. 74 X 138 d. 74 X 153

6. _ _ _ _ _ _ _ _ is 8 bit comparator and has no cascading inputs.

a. 74 X 85 b. 74 X 138 c. 74 X 682 d. 74 X 153

7. _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ is a synchronous 4 bit binary counter with active low load and clear input. { }

a. 74 × 163 b. 74 × 160 c. 74 × 74 d. 74 × 112

8. _ _ _ _ _ _ _ _ _ _ is a modulo 10 counter.

a. 74 × 112 b. 74 × 166 c. 74 × 74 d. 74 × 160

9. LFSR also known as { }

a. maximum length sequence generator

b. minimum length sequence generator

c. shift circular register

d. Johnson counter

10. _ _ _ _ _ _ _ _ _ _ _ _ _ is up/down counter. { }

a. 74 X 166 b. 74 X 169 c. 74 X 74 d. 74 X 112

11. _ _ _ _ _ _ _ _ _ _ _ _ _ is 8 bit serial in parallel out shift register. { }

a. GAL22V10 b. 74 X 74 c. 74 X 164 d. 74 X 112

Sign of Invigilator:

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL
III-YEAR I-SEM SECOND MID EXAMINATIONS – 05.03.2021
DIGITAL SYSTEM DESIGN
(Objective Type Test)

SET3

Date: 16 .11.2018 Max. Marks: 10
TIME: 20MIN BRANCH: ECE

1. For 74 X 151, input 0001 produces { }
a. D1 & not D1 b. D1 & not D2 c. D5 & not D5 d. D5 & not D6
2. _ _ _ _ _ _ _ _ _ _ _ is 2 input, 4 bit multiplexer. { }
a. 74 X 541 b. 74 X 157 c. 74 X 155 d. 74 X 148
3. 32 input, 1 bit multiplexer contains
a. 74 X 139, four 74 X 151 b. 74 X 136, two 74 X 151
c. 74 X 131, four 74 X 155 d. 74 X 130, four 74 X 159
4. _ _ _ _ _ _ is 9 bit parity generator. { }
a. 74 X 153 b. 74 X 86 c. 74 X 138 d. 74 X 280
5. _ _ _ _ _ _ _ _ has cascading inputs for combining multiple '85s to create comparator for more than four bits. { }
a. 74 X 85 b. 74 X 280 c. 74 X 138 d. 74 X 153
6. _ _ _ _ _ _ _ _ is 8 bit comparator and has no cascading inputs.
a. 74 X 85 b. 74 X 138 c. 74 X 682 d. 74 X 153
7. _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ is a synchronous 4 bit binary counter with active low load and clear input. { }
a. 74 × 163 b. 74 × 160 c. 74 × 74 d. 74 × 112
8. _ _ _ _ _ _ _ _ _ _ is a modulo 10 counter.
a. 74 × 112 b. 74 × 166 c. 74 × 74 d. 74 × 160
9. LFSR also known as { }
a. maximum length sequence generator
b. minimum length sequence generator
c. shift circular register
d. Johnson counter

10. _ _ _ _ _ _ _ _ _ _ _ _ is up/down counter. { }
a. 74 X 166 b. 74 X 169 c. 74 X 74 d. 74 X 112
11. _ _ _ _ _ _ _ _ _ _ _ _ is 8 bit serial in parallel out shift register. { }
a. GAL22V10 b. 74 X 74 c. 74 X 164 d. 74 X 112

12. _ _ _ _ _ _ _ _ _ _ _ _ is universal shift register. { }

a. 74 X 194 b. 74 X 166 c. 74 X 74 d. 74 X 112

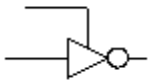
13. The IDLE output in generic 8 input priority encoder is asserted if _ _ _ _ _ are asserted.

a. no inputs b. I1, I4 c. I2,I6 d. I4,I5

14. _ _ _ _ _ _ _ must be asserted for any of its output to be asserted in 74 X 148 { }

a. EO _ H b. EO _ L c. EI _ L d. EI _ H

15. Shown in figure (a) represents { }



Figure(a)

a. Inverting active high enable buffer

b. Non - inverting active low enable buffer

c. inverting active low enable buffer

d. Non - inverting active high enable buffer

16. _ _ _ _ _ _ _ _ _ _ _ contains four independent Non - inverting three state buffer. { }

a. 74 X 120 b. 74 X 126 c. 74 X 129 d. 74 X 136

17. _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ is a synchronous 4 bit binary counter with active low load and clear input. { }

a. 74 × 163 b. 74 × 160 c. 74 × 74 d. 74 × 112

18. _ _ _ _ _ _ _ _ _ _ _ is a modulo 10 counter. { }

a. 74 × 112 b. 74 × 166 c. 74 × 74 d. 74 × 160

19. LFSR also known as { }

a. maximum length sequence generator

b. minimum length sequence generator

c. shift circular register

d. Johnson counter

20. _ _ _ _ _ _ _ _ _ _ _ _ is up/down counter. { }

a. 74 X 166 b. 74 X 169 c. 74 X 74 d. 74 X 112

12. _ _ _ _ _ _ _ _ _ _ _ is universal shift register. { }

a. 74 X 194 b. 74 X 166 c. 74 X 74 d. 74 X 112

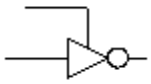
13. The IDLE output in generic 8 input priority encoder is asserted if _ _ _ _ _ are asserted.

a. no inputs b. I1, I4 c. I2,I6 d. I4,I5

14. _ _ _ _ _ _ _ must be asserted for any of its output to be asserted in 74 X 148 { }

a. EO _ H b. EO _ L c. EI _ L d. EI _ H

15. Shown in figure (a) represents { }



Figure(a)

a. Inverting active high enable buffer

b. Non - inverting active low enable buffer

c. inverting active low enable buffer

d. Non - inverting active high enable buffer

16. _ _ _ _ _ _ _ _ _ _ _ contains four independent Non - inverting three state buffer. { }

a. 74 X 120 b. 74 X 126 c. 74 X 129 d. 74 X 136

17. _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ is a synchronous 4 bit binary counter with active low load and clear input. { }

a. 74 × 163 b. 74 × 160 c. 74 × 74 d. 74 × 112

18. _ _ _ _ _ _ _ _ _ _ _ is a modulo 10 counter. { }

a. 74 × 112 b. 74 × 166 c. 74 × 74 d. 74 × 160

19. LFSR also known as { }

a. maximum length sequence generator

b. minimum length sequence generator

c. shift circular register

d. Johnson counter

20. _ _ _ _ _ _ _ _ _ _ _ _ is up/down counter. { }

a. 74 X 166 b. 74 X 169 c. 74 X 74 d. 74 X 112

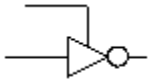
Sign of Invigilator:

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL
III-YEAR I-SEM SECOND MID EXAMINATIONS – 05.03.2021
DIGITAL SYSTEM DESIGN
(Objective Type Test)

SET4

Date: 16 .11.2018 Max. Marks: 10
TIME: 20MIN BRANCH: ECE

1. 74x682 does not provide { }
a. greater than output b. less than output
c. equal output d. output
2. if then else VHDL statement used within { }
a. WHILE b. select c. process d. assert
3. For more flexible comparisions & arithmetic operations IEEE 1076-3 created a package. it is { }
a. std logic arith b. std logic ulogic
c. std logic 1164 d. std logic unsigned
4. In 74 x 181, if S3 S2 S1 S0 = 1100, M = 1, then F is { }
a. 1001 b. 1010 c. 1111 d. 0000
5. _ _ _ _ _ _ _ _ specify the direction of shift, type of shift and amount of shift. { }
a. Barrel shifter b. Carry save shifter
c. sequential shifter d. group ripple shifter
6. _ _ _ _ _ _ _ _ _ _ contains four independent Non - inverting three state buffer. { }
a. 74 X 120 b. 74 X 126 c. 74 X 129 d. 74 X 136
7. Shown in figure (a) represents



Figure(a)

a. Inverting active high enable buffer
b. Non - inverting active low enable buffer
c. inverting active low enable buffer
d. Non - inverting active high enable buffer

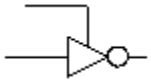
8. _ _ _ _ _ _ _ _ _ _ is octal Non - inverting three state buffer { }
a. 74 X 546 b. 74 X 451 c. 74 X 541 d. 74 X 544
9. _ _ _ _ _ _ _ _ _ is octal three state Trans receiver { }
a. 74 X 245 b. 74 X 254 c. 74 X 243 d. 74 X 241

Sign of Invigilator:

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN: KURNOOL
III-YEAR I-SEM SECOND MID EXAMINATIONS – 05.03.2021
DIGITAL SYSTEM DESIGN **SET4**
(Objective Type Test)

Date: 16 .11.2018 Max. Marks: 10
TIME: 20MIN BRANCH: ECE

1. 74x682 does not provide { }
a. greater than output b. less than output
c. equal output d. output
2. if then else VHDL statement used within { }
a. WHILE b. select c. process d. assert
3. For more flexible comparisions & arithmetic operations IEEE 1076-3 created a package. it is { }
a. std logic arith b. std logic ulogic
c. std logic 1164 d. std logic unsigned
4. In 74 x 181, if S3 S2 S1 S0 = 1100, M = 1, then F is { }
a. 1001 b. 1010 c. 1111 d. 0000
5. _ _ _ _ _ _ _ _ specify the direction of shift, type of shift and amount of shift. { }
a. Barrel shifter b. Carry save shifter
c. sequential shifter d. group ripple shifter
6. _ _ _ _ _ _ _ _ _ _ contains four independent Non - inverting three state buffer. { }
a. 74 X 120 b. 74 X 126 c. 74 X 129 d. 74 X 136
7. Shown in figure (a) represents



Figure(a)

a. Inverting active high enable buffer
b. Non - inverting active low enable buffer
c. inverting active low enable buffer
d. Non - inverting active high enable buffer

8. _ _ _ _ _ _ _ _ _ _ is octal Non - inverting three state buffer { }
a. 74 X 546 b. 74 X 451 c. 74 X 541 d. 74 X 544
9. _ _ _ _ _ _ _ _ _ is octal three state Trans receiver { }
a. 74 X 245 b. 74 X 254 c. 74 X 243 d. 74 X 241

10. _ _ _ _ _ _ _ _ _ in 74 X 245 determines direction of transfer { }

a. G L b. G1 L c. G2 L d. dir

11. _ _ _ _ _ _ _ _ _ _ is 6 bit register. { }

a. 74 × 174 b. 74 × 375 c. 74 × 75 d. 74 × 112

12. _ _ _ _ _ _ _ _ _ _ is (octal edge trigger D FF) 8 bit register. { }

a. 74 × 174 b. 74 × 74 c. 74 × 374 d. 74 × 112

13. _ _ _ _ _ _ _ _ _ _ uses D latches. { }

a. 74 × 373 b. 74 × 174 c. 74 × 74 d. 74 × 112

14. _ _ _ _ _ _ _ _ _ _ _ _ uses pin 1 for asynchronous clear input. { }

a. 74 × 273 b. 74 × 174 c. 74 × 74 d. 74 × 112

15. _ _ _ _ _ _ _ _ _ _ _ _ uses pin1 for active low clock enable input. { }

a. 74 × 174 b. 74 × 377 c. 74 × 74 d. 74 × 112

16. A 1M X 1 ROM could be built with { }

a. 3 to 8 decoder and 16 input multiplexer

b. floating source MOS

c. 10 to 1024 decoder and 1024 input multiplexer

d. 3 to 10 decoder and 20 input multiplexer

17. _ _ _ _ _ _ _ _ _ _ _ is used to reduce the decoder size in ROM { }

a. one dimensional decoding

b. Two dimensional decoding

c. five dimensional decoding

d. four dimensional decoding

18. EEPROM (NMOS Technology) Read cycle is { }

a. 500 - 1500ns b. 250 -1 200ms c. 250 - 300ns d. 50 - 200 ns

19. EPROMs will have { }

a. floating gate MOS

b. floating source MOS

c. floating drain MOS

d. floating body MOS

20. _ _ _ _ _ _ _ _ _ _ is 8K X 8 EPROM. { }

a. 2764 b. HM6264 c. 74 X 74 d. 74 X 112

10. _ _ _ _ _ _ _ _ _ in 74 X 245 determines direction of transfer { }

a. G L b. G1 L c. G2 L d. dir

11. _ _ _ _ _ _ _ _ _ _ is 6 bit register. { }

a. 74 × 174 b. 74 × 375 c. 74 × 75 d. 74 × 112

12. _ _ _ _ _ _ _ _ _ _ is (octal edge trigger D FF) 8 bit register. { }

a. 74 × 174 b. 74 × 74 c. 74 × 374 d. 74 × 112

13. _ _ _ _ _ _ _ _ _ _ uses D latches. { }

a. 74 × 373 b. 74 × 174 c. 74 × 74 d. 74 × 112

14. _ _ _ _ _ _ _ _ _ _ _ _ uses pin 1 for asynchronous clear input. { }

a. 74 × 273 b. 74 × 174 c. 74 × 74 d. 74 × 112

15. _ _ _ _ _ _ _ _ _ _ _ _ uses pin1 for active low clock enable input. { }

a. 74 × 174 b. 74 × 377 c. 74 × 74 d. 74 × 112

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d. 3 to 10 decoder and 20 input multiplexer

17. _ _ _ _ _ _ _ _ _ _ _ is used to reduce the decoder size in ROM { }

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18. EEPROM (NMOS Technology) Read cycle is { }

a. 500 - 1500ns b. 250 -1 200ms c. 250 - 300ns d. 50 - 200 ns

19. EPROMs will have { }

a. floating gate MOS

b. floating source MOS

c. floating drain MOS

d. floating body MOS

20. _ _ _ _ _ _ _ _ _ _ is 8K X 8 EPROM. { }

a. 2764 b. HM6264 c. 74 X 74 d. 74 X 112

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN(3T), KURNOOL

B.Tech – III-I Semester (R15) MID II Examinations

Branch: ECE

SET- 1

Sub: DSD **Date:- 05.03.2021**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Write a VHDL program for 2 x 4 Decoder.	**2**	**3**	C303.2	Understand
ii)	Write modes of operation of shift registers.	**2**	**4**	C303.1	Analyze
iii)	Write a VHDL code for 3-bit ring counter.	**2**	**4**	C303.3	Remember
iv)	Explain about parallel in serial out shift register.	**2**	**5**	C303.3	Remember
v)	What are the applications of flip flops?	**2**	**5**	C303.1	Remember
2. a)	Design a priority encoder for 16 inputs using two 74 × 14 encoders.	**6**	**3**	C303.1	Understand
b)	Compare PROM, PAL and PLA.	**4**	**3**	C303.1	Understand
3.a)	Design an 8-bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.	**5**	**4**	C303.2	Understand
b)	Explain in detail about the working of Johnson Counter using 74 LS194.	**5**	**5**	C303.2	Evaluate
4.a)	Design a 3-bit synchronous up counter using T Flip-flops.	**5**	**4**	C303.3	Understand
b)	Explain the design of a 4-bit binary counter with Parallel load in detail.	**5**	**5**	C303.3	Understand
5.a)	Draw the block diagram and explain in detail about the PAL.	**5**	**5**	C303.3	Understand
b)	Write Verilog module for 8-bit comparator with test bench.	**5**	**5**	C303.3	Remember

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN(3T), KURNOOL

B.Tech – III-I Semester (R15) MID II Examinations

Branch: ECE

SET- 1

Sub: DSD **Date:- 05.03.2021**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Write a VHDL program for 2 x 4 Decoder.	**2**	**3**	C303.2	Understand
ii)	Write modes of operation of shift registers.	**2**	**4**	C303.1	Analyze
iii)	Write a VHDL code for 3-bit ring counter.	**2**	**4**	C303.3	Remember
iv)	Explain about parallel in serial out shift register.	**2**	**5**	C303.3	Remember
v)	What are the applications of flip flops?	**2**	**5**	C303.1	Remember
2. a)	Design a priority encoder for 16 inputs using two 74 × 14 encoders.	**6**	**3**	C303.1	Understand
b)	Compare PROM, PAL and PLA.	**4**	**3**	C303.1	Understand
3.a)	Design an 8-bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.	**5**	**4**	C303.2	Understand
b)	Explain in detail about the working of Johnson Counter using 74 LS194.	**5**	**5**	C303.2	Evaluate
4.a)	Design a 3-bit synchronous up counter using T Flip-flops.	**5**	**4**	C303.3	Understand
b)	Explain the design of a 4-bit binary counter with Parallel load in detail.	**5**	**5**	C303.3	Understand
5.a)	Draw the block diagram and explain in detail about the PAL.	**5**	**5**	C303.3	Understand
b)	Write Verilog module for 8-bit comparator with test bench.	**5**	**5**	C303.3	Remember

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN(3T), KURNOOL

B.Tech – III-I Semester (R15) MID II Examinations

Branch: ECE

SET- 2

Sub: DSD **Date:- 05.03.2021**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Compare PAL and PLA.	**2**	**3**	C303.1	Remember
ii)	Draw the state diagram of modulo-4 up/down counter.	**2**	**4**	C303.1	Understand
iii)	Discuss the steps involved in the analysis of sequential circuits.	**2**	**4**	C303.3	Understand
iv)	List out basic types of programmable logic devices.	**2**	**5**	C303.3	Remember
v)	Draw the circuit diagram of 3-bit bidirectional shift register.	**2**	**5**	C303.2	Remember
2. a)	With neat diagram, explain 3 to 8-line decoder.	**5**	**3**	C303.2	Remember
b)	Design a two-bit comparator circuit and explain its operation.	**5**	**3**	C303.1	Remember
3.a)	Design a self-correcting 4-bit, 4-state ring counter with a single circulating using IC 74LS194.	**5**	**4**	C303.3	Understand
b)	With a neat sketch, explain the Universal shift register.	**5**	**4**	C303.3	Understand
4.a)	What is a floating-point encoder? Explain	**5**	**5**	C303.3	Understand
b)	Write VHDL code for 4 bit Barrel Shifter.	**5**	**5**	C303.3	Remember
5.a)	What is a PLD? Compare the three combinational PLDs?	**5**	**5**	C303.3	Understand
b)	Discuss the logic circuit of 74 × 377 register. Write a VHDL program for the same in structural style.	**5**	**3**	C303.3	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN(3T), KURNOOL

B.Tech – III-I Semester (R15) MID II Examinations

Branch: ECE

SET- 2

Sub: DSD **Date:- 05.03.2021**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Compare PAL and PLA.	**2**	**3**	C303.1	Remember
ii)	Draw the state diagram of modulo-4 up/down counter.	**2**	**4**	C303.1	Understand
iii)	Discuss the steps involved in the analysis of sequential circuits.	**2**	**4**	C303.3	Understand
iv)	List out basic types of programmable logic devices.	**2**	**5**	C303.3	Remember
v)	Draw the circuit diagram of 3-bit bidirectional shift register.	**2**	**5**	C303.2	Remember
2. a)	With neat diagram, explain 3 to 8-line decoder.	**5**	**3**	C303.2	Remember
b)	Design a two-bit comparator circuit and explain its operation.	**5**	**3**	C303.1	Remember
3.a)	Design a self-correcting 4-bit, 4-state ring counter with a single circulating using IC 74LS194.	**5**	**4**	C303.3	Understand
b)	With a neat sketch, explain the Universal shift register.	**5**	**4**	C303.3	Understand
4.a)	What is a floating-point encoder? Explain	**5**	**5**	C303.3	Understand
b)	Write VHDL code for 4 bit Barrel Shifter.	**5**	**5**	C303.3	Remember
5.a)	What is a PLD? Compare the three combinational PLDs?	**5**	**5**	C303.3	Understand
b)	Discuss the logic circuit of 74 × 377 register. Write a VHDL program for the same in structural style.	**5**	**3**	C303.3	Understand

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN(3T), KURNOOL

B.Tech – III-I Semester (R15) MID II Examinations

Branch: ECE

SET- 3

Sub: DSD **Date:- 05.03.2021**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Compare decoder and de multiplexer.	**2**	**3**	C303.2	Analyze
ii)	Design a half subtractor.	**2**	**3**	C303.2	Remember
iii)	Convert T Flip Flop to D Flip Flop.	**2**	**4**	C303.3	Remember
iv)	What is the difference between asynchronous And synchronous sequential circuits?	**2**	**4**	C303.3	Remember
v)	Compare latches and flip-flops.	**2**	**5**	C303.3	Remember
2.a)	Elaborate the concept of PROM, EPROM, EEPROM in detail.	**3**	**10**	C303.3	understand
3.a)	Design a 3-bit bidirectional shift register.	**4**	**10**	C303.3	Analyze
4.a)	Explain ring counter with its logic diagram.	**4**	**5**	C303.2	understand
b)	Write a VHDL program for a 8-bit comparator.	**5**	**5**	C303.2	understand
5.a)	Explain about combinational multipliers"	**3**	**3**	C303.3	Create
b)	Describe dual parity encoder.	**5**	**2**	C303.3	Analyze

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN(3T), KURNOOL

B.Tech – III-I Semester (R15) MID II Examinations

Branch: ECE

SET- 3

Sub: DSD **Date:- 05.03.2021**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	Compare decoder and de multiplexer.	**2**	**3**	C303.2	Analyze
ii)	Design a half subtractor.	**2**	**3**	C303.2	Remember
iii)	Convert T Flip Flop to D Flip Flop.	**2**	**4**	C303.3	Remember
iv)	What is the difference between asynchronous And synchronous sequential circuits?	**2**	**4**	C303.3	Remember
v)	Compare latches and flip-flops.	**2**	**5**	C303.3	Remember
2.a)	Elaborate the concept of PROM, EPROM, EEPROM in detail.	**3**	**10**	C303.3	understand
3.a)	Design a 3-bit bidirectional shift register.	**4**	**10**	C303.3	Analyze
4.a)	Explain ring counter with its logic diagram.	**4**	**5**	C303.2	understand
b)	Write a VHDL program for a 8-bit comparator.	**5**	**5**	C303.2	understand
5.a)	Explain about combinational multipliers"	**3**	**3**	C303.3	Create
b)	Describe dual parity encoder.	**5**	**2**	C303.3	Analyze

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN(3T), KURNOOL

B.Tech – III-I Semester (R15) MID II Examinations

Branch: ECE

SET-4

Sub: DSD **Date:- 05.03.2021**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

		Marks	Unit	CO	Cognitive Level
1. i)	What is PLA?	**2**	**3**	C303.1	Remember
ii)	What is a combinational PLD?	**2**	**4**	C303.3	Remember
iii)	What is a shift register?	**2**	**4**	C303.1	Remember
iv)	What is Johnson counter?	**2**	**5**	C303.2	Remember
v)	What is timing verification?	**2**	**5**	C303.3	Remember
2. a)	Implement 4-bit ripple adder using 1-bit full adder and write VHDL code for this implementation.	**5**	**3**	C303.1	understand
b)	Explain the operation of comparators and write VHDL code for the corresponding.	**5**	**3**	C303.2	understand
3.a)	Write VHDL code for 4-bit up-down counter with synchronous reset and clear inputs.	**5**	**4**	C303.1	understand
b)	Explain the working of ring counter and write VHDL code for 4-bit ring counter.	**5**	**4**	C303.1	understand
4.a)	Explain the difference between D-latch and D-Flip-flop using the process block in VHDL.	**5**	**5**	C303.3	understand
(b)	Explain the operation of dual parity encoder and writea VHDL code for the corresponding.	**5**	**5**	C303.3	Create
5.	Define state, state diagram. Draw state diagram taking any one as an example.	**5**	**4**	C303.3	Evaluate
b.)	Design MOD-16 synchronous counter using T- Flip-Flop.	**5**	**4**	C303.3	Create

RAVINDRA COLLEGE OF ENGINEERING FOR WOMEN(3T), KURNOOL

B.Tech – III-I Semester (R15) MID II Examinations

Branch: ECE

SET-4

Sub: DSD **Date:- 05.03.2021**

Time: 1½ Hrs. **Max Marks: 30M**

Question 1 is compulsory. Answer one from 2 or 3 and one from 4 or 5.

.

		Marks	Unit	CO	Cognitive Level
1. i)	What is PLA?	**2**	**3**	C303.1	Remember
ii)	What is a combinational PLD?	**2**	**4**	C303.3	Remember
iii)	What is a shift register?	**2**	**4**	C303.1	Remember
iv)	What is Johnson counter?	**2**	**5**	C303.2	Remember
v)	What is timing verification?	**2**	**5**	C303.3	Remember
2. a)	Implement 4-bit ripple adder using 1-bit full adder and write VHDL code for this implementation.	**5**	**3**	C303.1	understand
b)	Explain the operation of comparators and write VHDL code for the corresponding.	**5**	**3**	C303.2	understand
3.a)	Write VHDL code for 4-bit up-down counter with synchronous reset and clear inputs.	**5**	**4**	C303.1	understand
b)	Explain the working of ring counter and write VHDL code for 4-bit ring counter.	**5**	**4**	C303.1	understand
4.a)	Explain the difference between D-latch and D-Flip-flop using the process block in VHDL.	**5**	**5**	C303.3	understand
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b.)	Design MOD-16 synchronous counter using T- Flip-Flop.	**5**	**4**	C303.3	Create