Unit V

- **Digital Logic Families: Unipolar and Bipolar Logic Families, Transistor-Transistor Logic (TTL): Operation of TTL, Current sink logic, TTL with active pull up, TTL with open collector output,** Shockley TTL, TTL characteristics, I2L, ECL logic Families.
- **CMOS:** CMOS Inverter, CMOS characteristics, CMOS configurations - Wired Logic, Open drain outputs, Interfacing: TTL to CMOS and CMOS to TTL, Tristate Logic, Characteristics of Digital ICs: Speed, power dissipation, figure of merit, fan-out, Current and voltage parameters, Noise immunity, operating temperature range, power supply requirements.

INTRODUCTION

- Digital logic is concerned with the interconnection among digital components and modules. The best known example of a digital system is the general purpose digital computer. Most of the digital circuits are constructed on a single chip, which are referred to as integrated circuits (IC).
- Integrated circuits contain a large number of interconnected digital circuits within a single small package.
- Small scale integration (SSI)
- Medium scale integration (MSI)
- Large scale integration (LSI)
- Very Large Scale Integration (VLSI)

Name	Signification	Number of Transistors
SSI	Small-Scale Integration	1 to 10
MSI	Medium-Scale Integration	10 to 500
LSI	Large-Scale Integration	500 to 20,000
VLSI	Very Large-Scale Integration	20,000 to 1,000,000
ULSI	Ultra Large-Scale Integration	more than 1,000,000

Generations of Integrated Circuits

Introduction…continued

- Based on the fabrication technology, logic families are classified into two types: Bipolar logic family and Unipolar logic family.

- Unipolar Logic Family: In unipolar logic families, unipolar devices are the key element. MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a unipolar device, in which the current flows because of only one type of charge carriers (that is, either electrons or holes). The examples of unipolar families include PMOS, NMOS, and CMOS

- Bipolar Logic Family: Transistors and diodes are bipolar devices, in which the current flows because of both the charge carriers (electrons and holes). In bipolar logic families, transistors and diodes are used as key element.

Characteristics of Digital ICs

There are various logic families and the selection of a family for a particular application is based on its characteristics:

Following are the parameters used to compare the performance of digital ICs:

- Speed
- Power dissipation
- Figure of merit
- Fan-out
- Current and voltage parameters
- Noise immunity
- Operating temperature range
- Power supply requirements.

Characteristics of Digital ICs

Operating Speed: Speed of a logic gate depends upon the time that elapses between the application of a signal to an input terminal and the resulting change in logical state at the output terminals. It takes into consideration the transition time (rise and fall duration of a pulse) and propagation delays. Both of these times depend upon the loading and increase with increase in load. The more inputs are attached to the output of a logic gate, the more load is to be handled by that output. high operating speed is usually the main requirement of digital ICs.

Power Dissipation: This is the amount of power dissipated in an IC. It is determined by the current, Icc. that it draws from the Vcc supply and equals Vcc Icc where Icc is average value of Icc(0) and Icc(1). This power is specified in mW. Lower power dissipation is desirable feature for any IC.

Fan-In: The fan-in of a logic gate is defined as the number of inputs (coming from similar circuits) that it can handle properly.

Fan-Out: In general, a logic circuit is required to drive several logic inputs. The fan-out (also sometimes called the loading factor) is defined as the maximum number of standard logic inputs that an output can drive reliably. For example, a logic gate that is specified to have a fan-out of 8 can drive 8 standard logic inputs. if this number exceeds the output logic-level voltages cannot be guaranteed.

Operating Temperature Range: Digital ICs should be capable of operating for temperature ranging from 0^0Cto 70^0C for consumers and from -55^0C to $+125^0$C for military applications.

Characteristics of Digital ICs

Power Supply Requirements: Every IC requires a certain amount of electrical power to operate. The power is supplied by one or more power-supply voltage connected to the power pin (or pins) on the chip. Usually there is only one power-supply terminal on the chip ans it is marked Vcc for TTL or VDD for for MOS devices. Obviously low power consumption is desirable features in any digital ICs.

Figure of merit = Propagation time (ns) x power (mW) [Measured in pico joules (pJ)]

A low value of speed-power product is desirable. In a digital circuit if high speed or low propogation delay is desired, then there will be corresponding increase in power dissipation and vice-versa.

Noise Immunity: Stray electric and magnetic fields can induced voltages on the connecting wires between logic circuits. these unwanted, spurious signals are known as noise and can sometimes lead to false triggering of logic levels in the circuits. The noise immunity of a logic circuit refers to the circuits's ability to tolerate noise voltages on its inputs. A quantitative measure of noise margin. Higher the noise margin, better the logic cirucit.

Figure of Merit: The figure of merit of a digital IC is defined as the product of speed and power. The speed is specified in terms of propagation delay time expressed in nano seconds.

Propagation Delay

- ★ Due finite switching speed of transistors and circuit capacitances
- ★ tPHL: Delay in changing output from H to L
- ★ tPLH: Delay in changing output from L to H
- ★ Propagation delay, tPD= (tPHL+ tPLH)/2
- ★ tr: Rise time 10% to 90% of max.
- ★ tf: Fall time 90% to 10% …

Power dissipation

Static power dissipation

-when transistor is either ON or OFF

-depends on current drawn in each case

-power dissipation, P_D is average of these two

-significant in switching of Bipolar Junction Transistor

Dynamic power dissipation

-when transistor switches

-depends on switching speed

-significant in switching of CMOS Transistor

Figure of Merit,

$F = P_D \times t_{PD}$

The lower the F, the better.

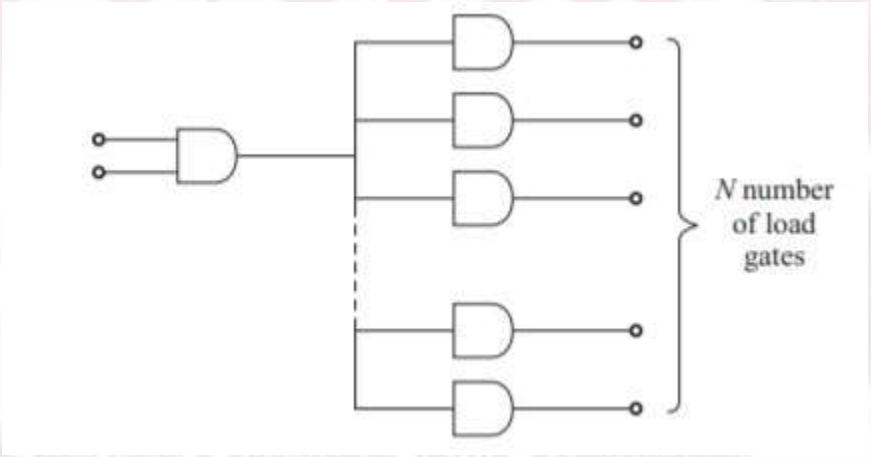
Noise Immunity

Unwanted signals are known **as noise.** The stray electric and magnetic fields may induce some noise at an input of digital circuit. Because of noise, the input voltage may drop which results in undesired operations. The circuit should have the ability to tolerate the noise signal.

The noise immunity of digital circuit is defined as the ability of a digital circuit to tolerate the noise signal.

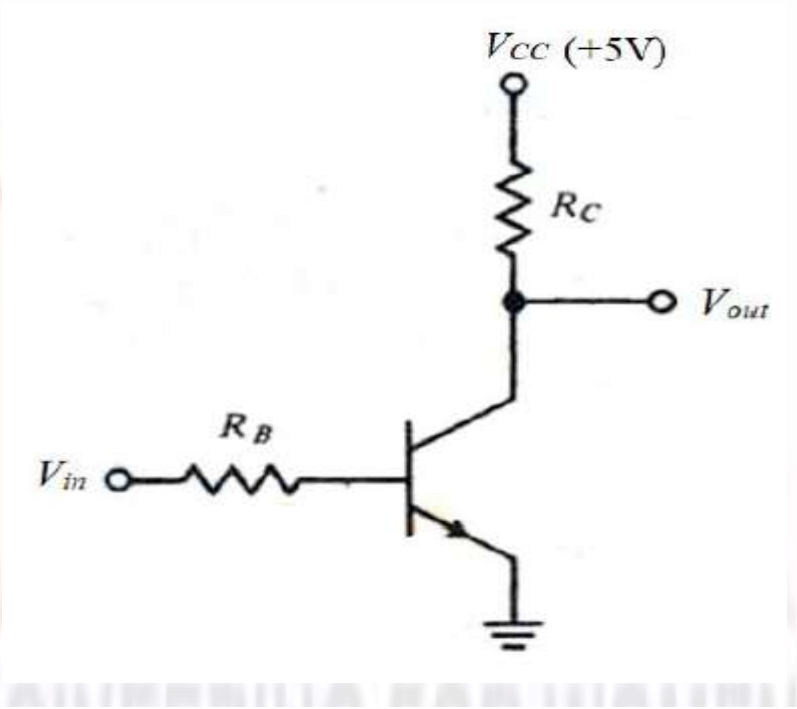
A quantitative measure of noise immunity is known as **noise margin**.

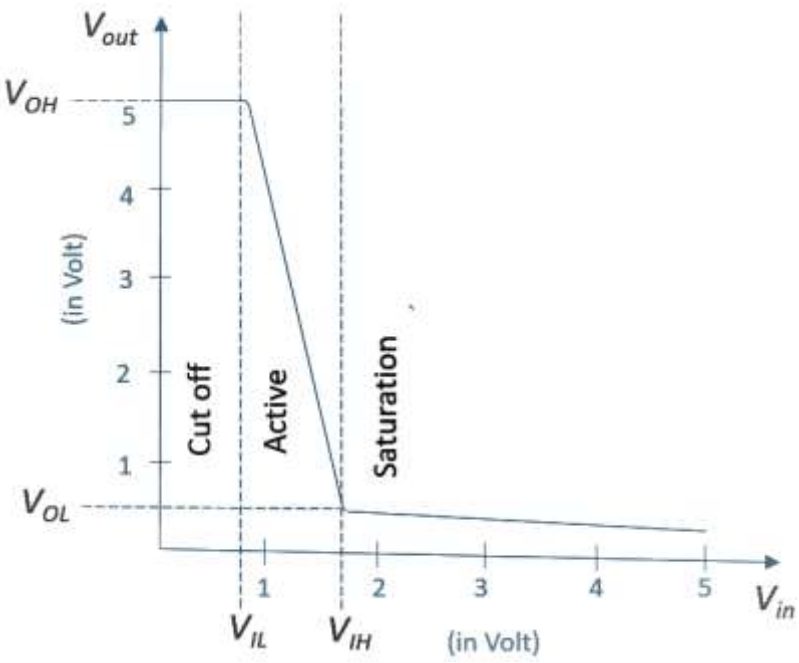
Fig : Fan out ; AND gate driving N gates



Transistor as a switch

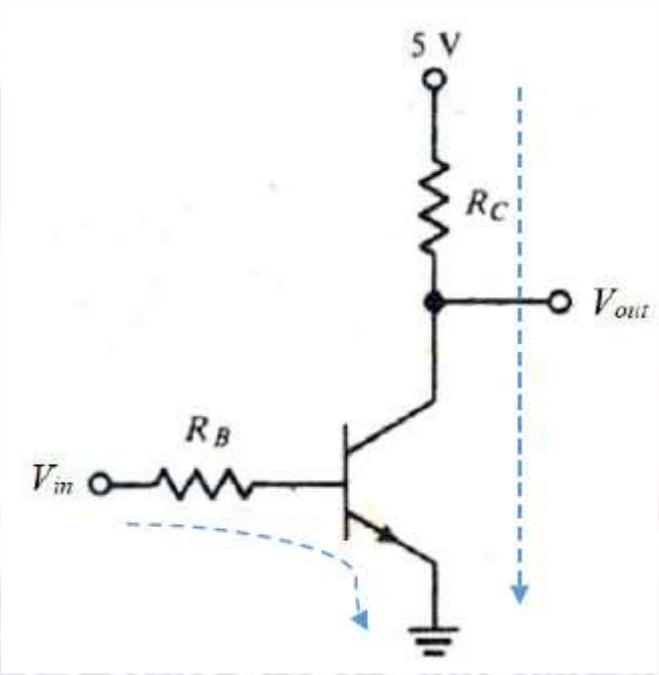
- **Cut-off region**
- **Base current IB= 0 till VBE< 0.7V i.e. Vin< 0.7V.**
- **Transistor is *cut off* and IC= 0 with Vout= 5V over entire range.**
- **When Vin is increased beyond 0.7V, base current begins to flow and the transistor moves from *cut off* region to *normal active* region.**
- **The coordinate, Vin= 0.7V, Vout= 5V mark first transition point in the transfer function of this circuit. This is also termed as *break point* or *edge of cutoff* (EOC).**





Transistor as a switch

- ★ **Active region**
- ★ **Applying KVL along Vin, RB, VBE, Ground**



IB= (Vin–VBE(on))/RB

- ★ **In active region, IC= βFIB(as long as VCE< VCE(sat))**
- ★ **Applying KVL along Vcc, RC, VCE, Ground**

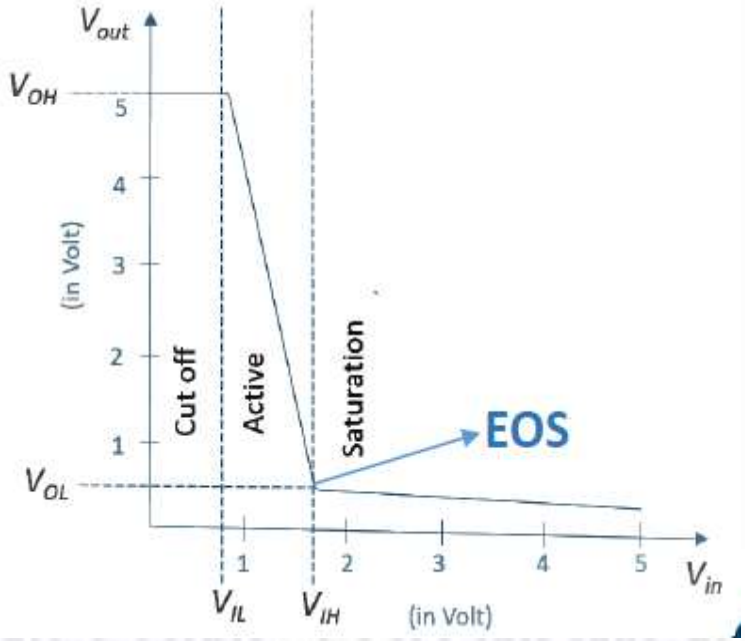
Vout= VCC-ICRC= VCC-βFIBRC

- ★ **Combining,**

Vout= VCC-βFRC(Vin–VBE(on))/RB

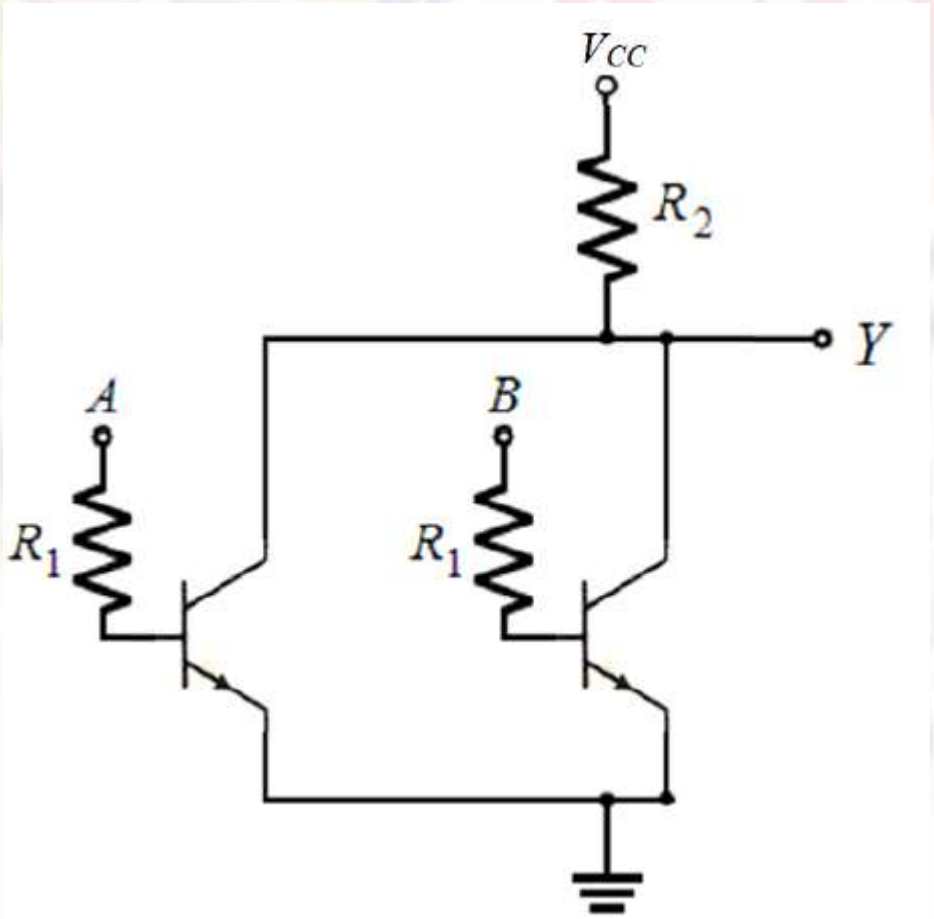
Transistor as a switch

- **Saturation region**
- As Vin(or IB) is increased a second transition point is reached when Vout= VCE(sat).
- The values of ICand IBfor this condition (the subscript EOS means *edge of saturation*):
- IC(EOS)= (VCC–VCE(sat))/RC= (5-0.2)/1 = 4.8mA
- and IB(EOS)= IC(EOS)/βF= 4.8/50 = 0.096mA
- Then Vin(EOS)= VBE(on)+ IB(EOS)RB= 0.7 + (0.096)(10) = 1.66V
- Thus Vin≥1.66V the transistor saturates. (Saturating Logic)



RTL: Resistance Transistor Logic

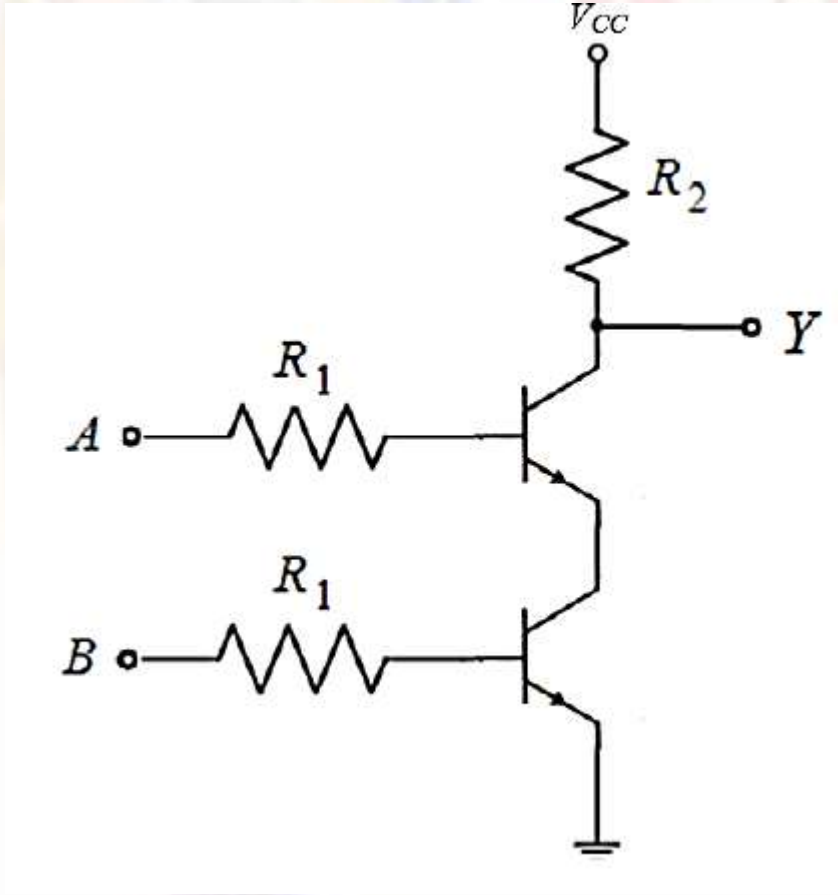
★ **RTL NOR Gate**



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

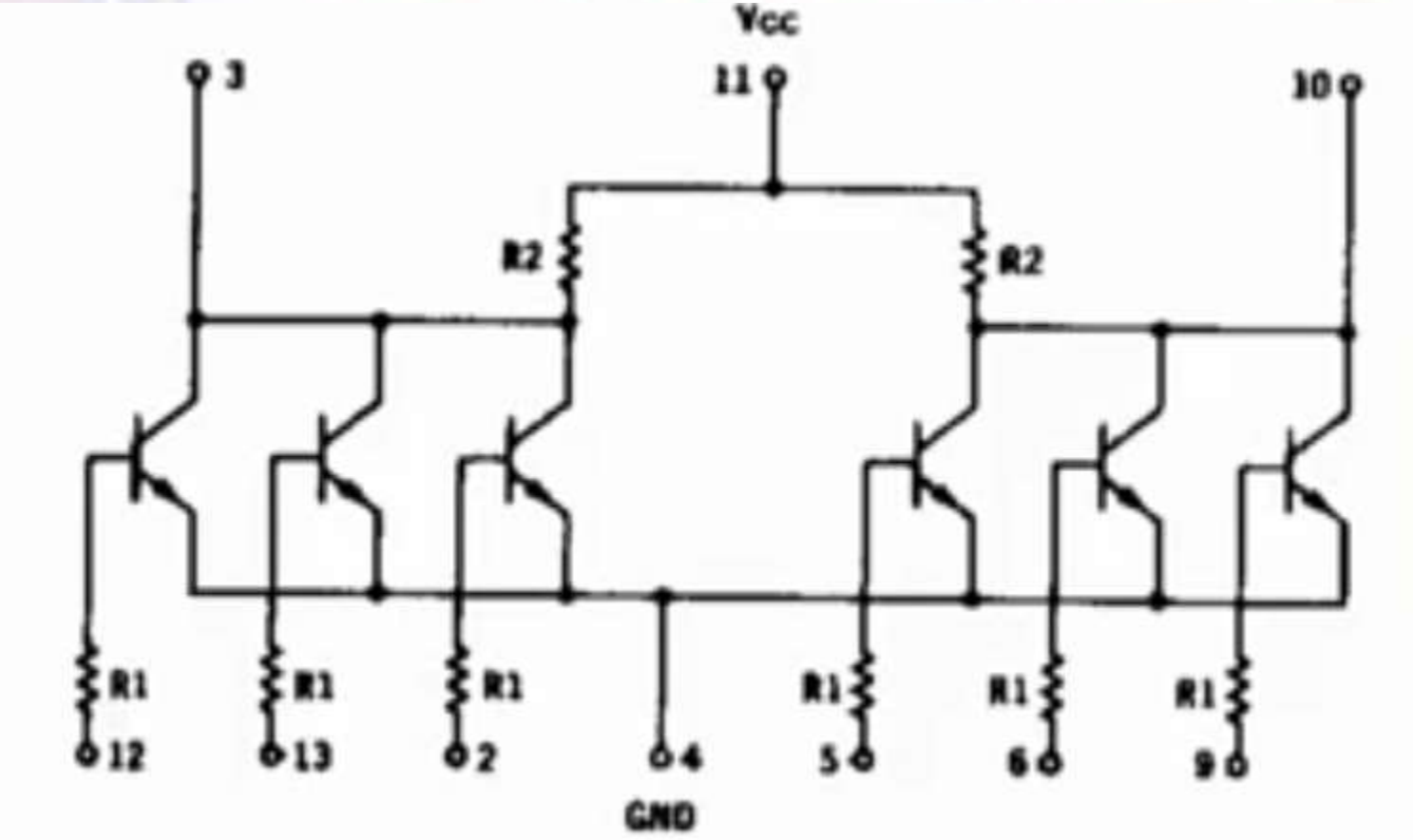
RTL: Resistance Transistor Logic

- ★ **RTL NAND Gate**
- ★ **It will be shown that any other logic gates can be obtained using only NAND gate or NOR gate.**



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Home Work

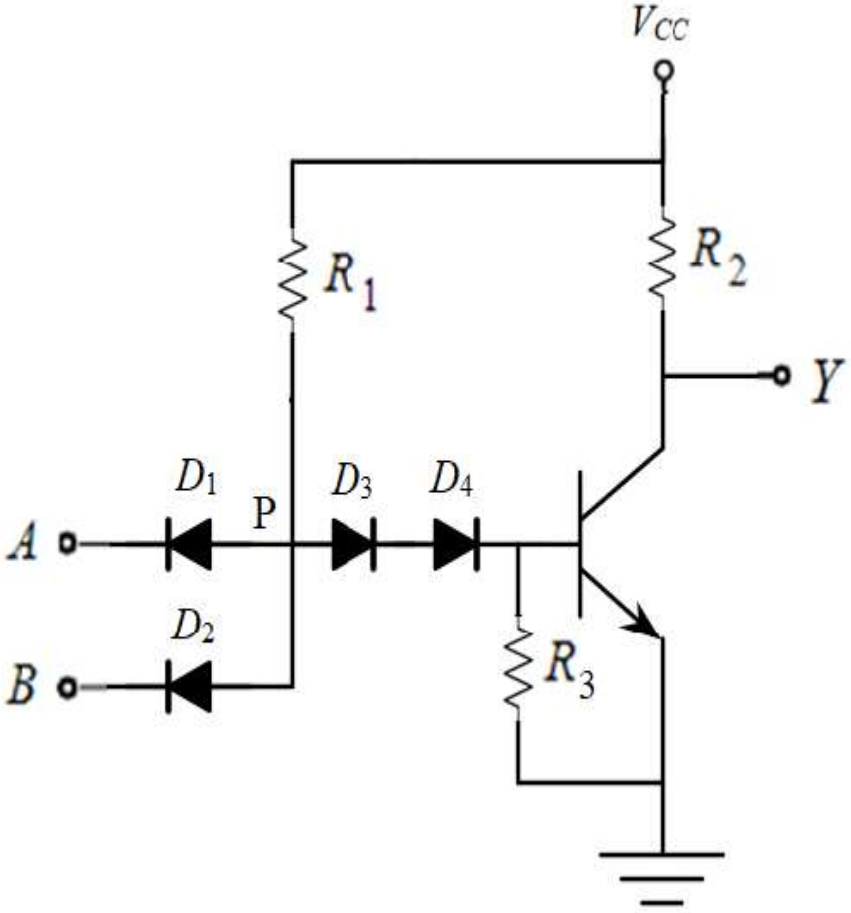


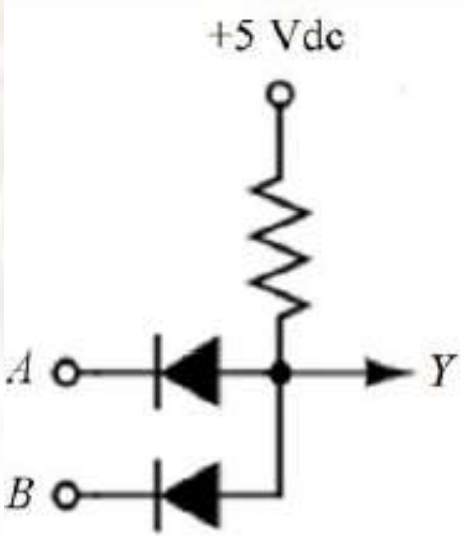
★ **Explain the operation of the circuit and draw the truth table**

Two 3-input NOR gates ; R1 = 450Ω, R2 = 640Ω; PD= 55 mW(input H), 15 mW(input L) tPD= 12 ns

DTL: Diode Transistor Logic

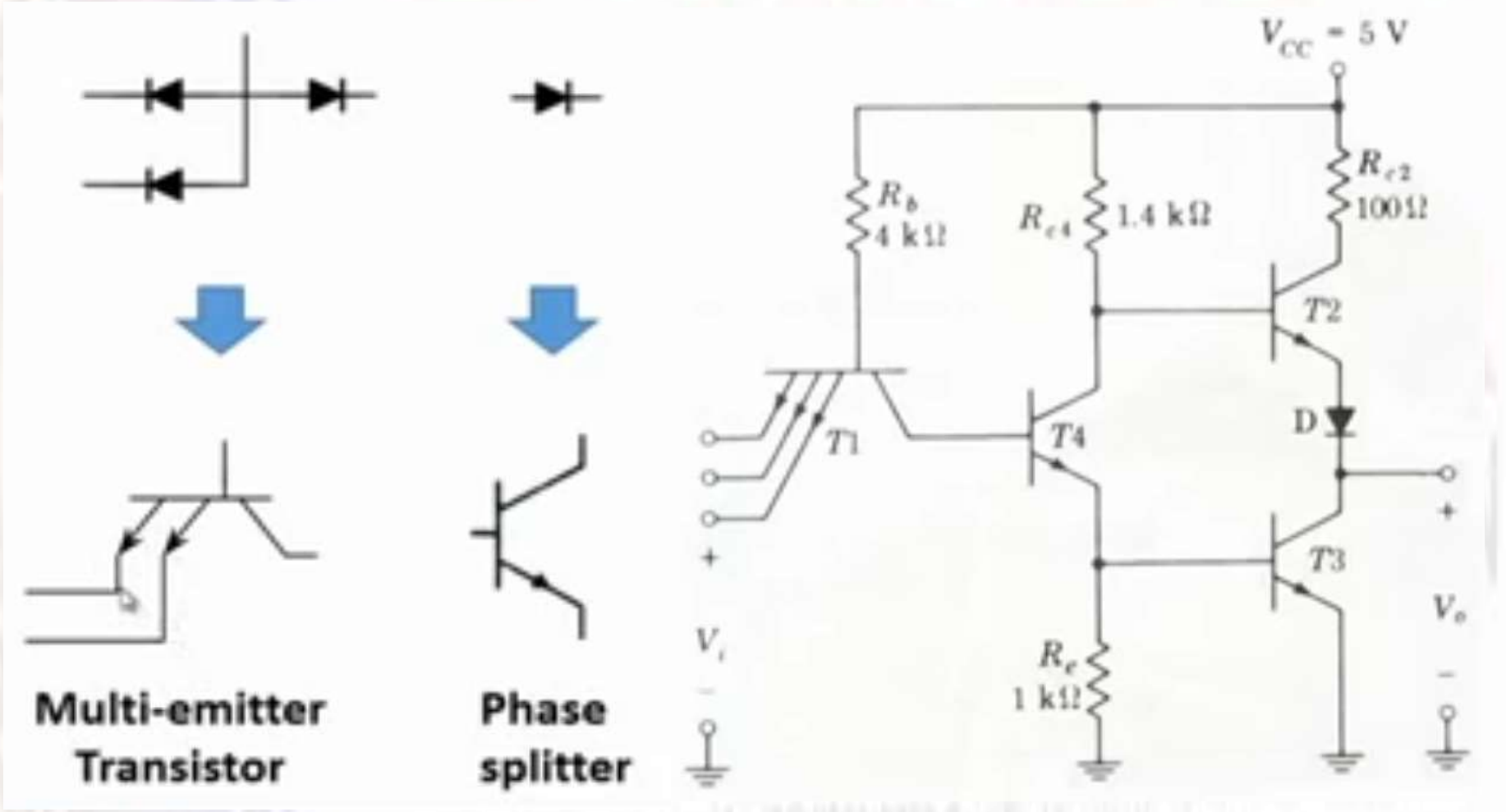
- ★ DTL NAND Gate
- ★ D1, D2, R1, VCC: AND logic at P.
- ★ D3 and D4 are level shifters ; (VP= 3 x 0.7V turns ON transistor.)
- ★ R3 provides discharge path of stored charge at BE junction that reduces tPLH.
- ★ Any of A or B low (0.2 V), VP= 0.9 V, insufficient to turn ON the transistor.



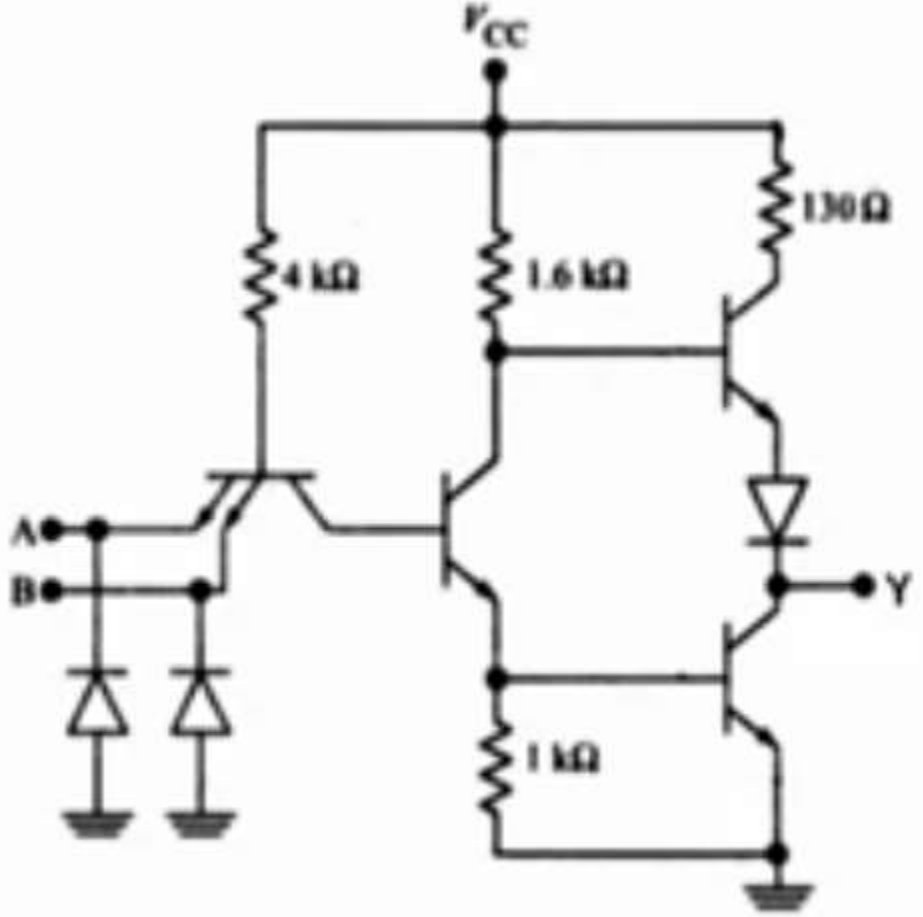


A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

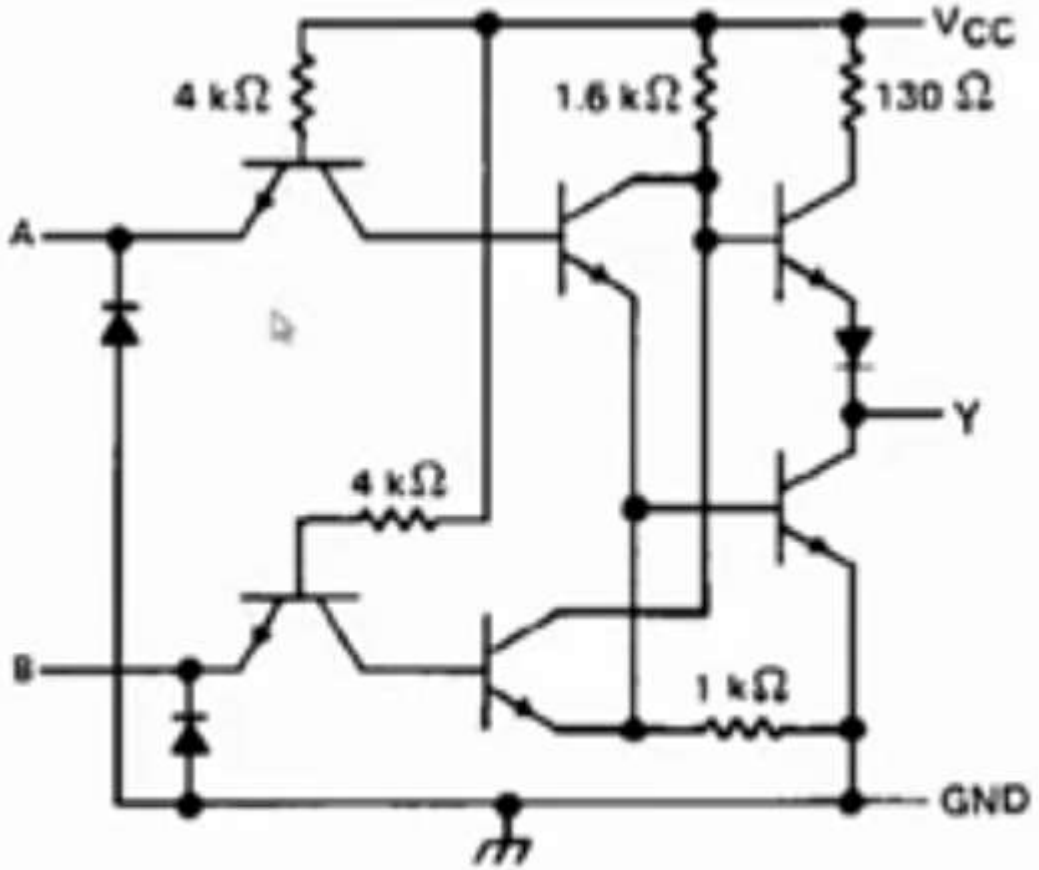
TTL: Transistor Transistor Logic
NAND Gate



- ★ Totem pole output reduces output resistance when at H.
- ★ R3 cannot be made zero.
- ★ D1 to avoid indeterminate output.

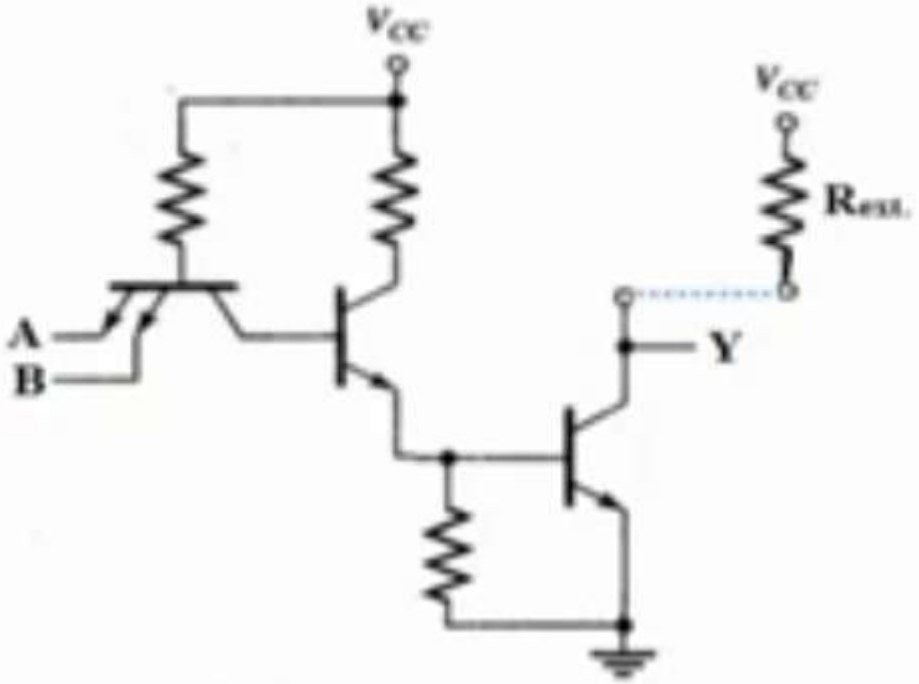


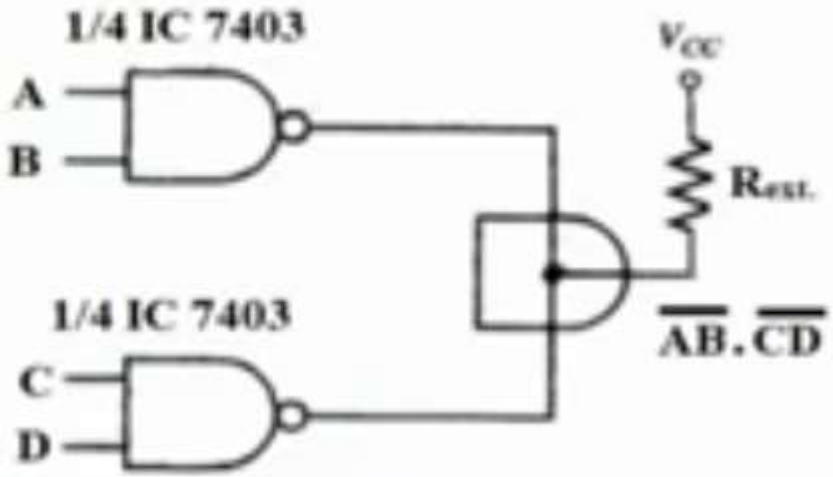
2-input NAND gate



From TI SN7402 (2-input NOR) datasheet

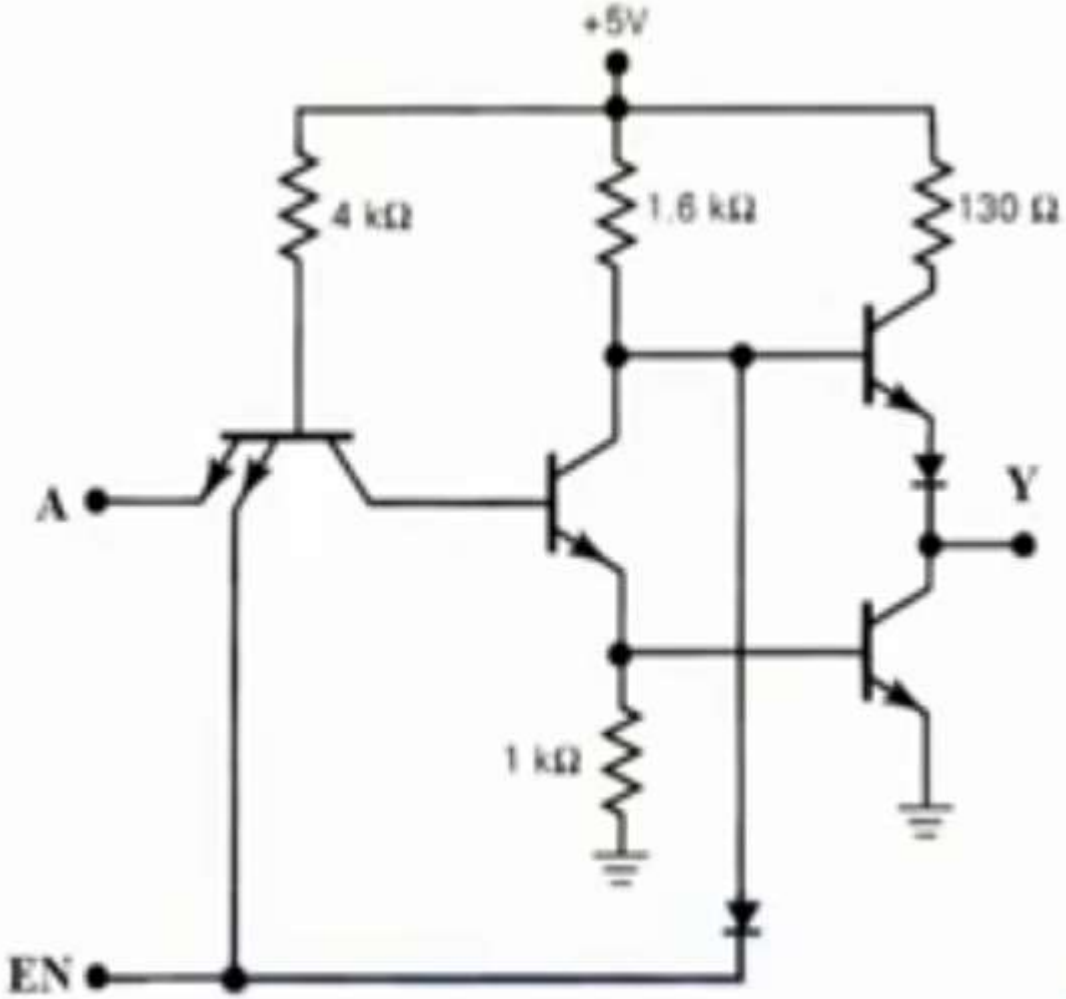
TTL with open Collector output

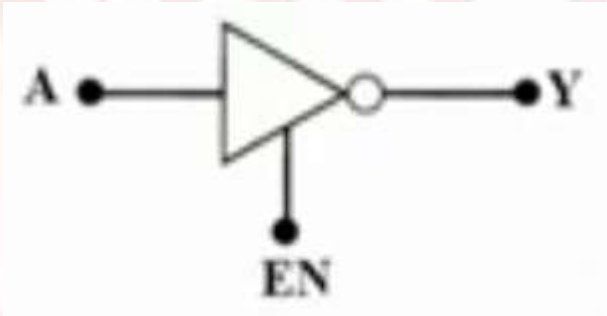




It is not working with open collector, so, connect a resistor t make it operation. By varying the resistor, current flow can be controlled.

TTL Tristate

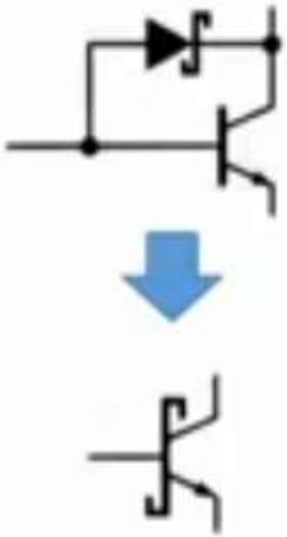


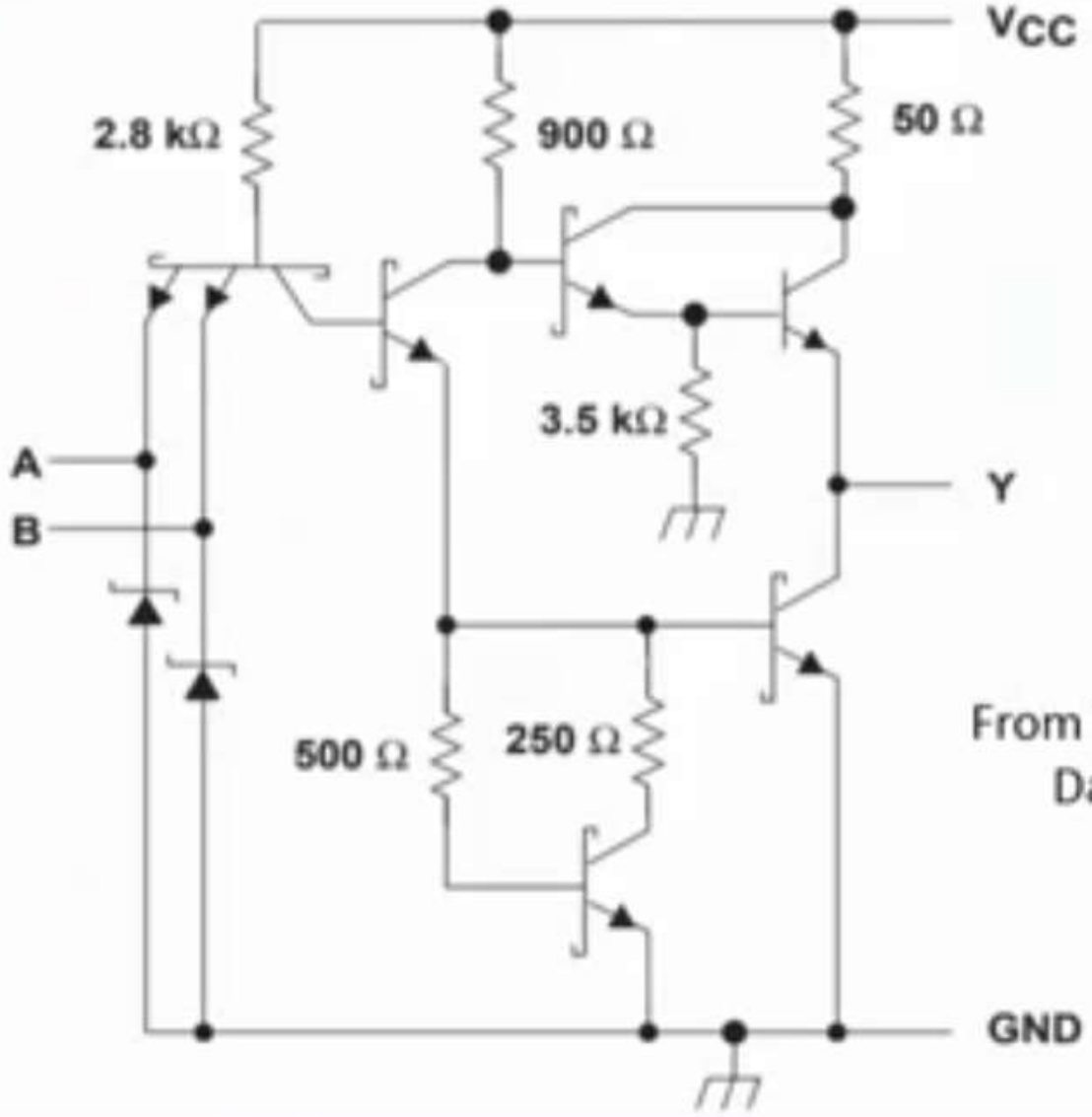


When EN =0, First two transistors are off and third transistor may be on, but due to diode, it may not able to turn on, so both output transistors are off, which is tri-state condition.

Schottky TTL

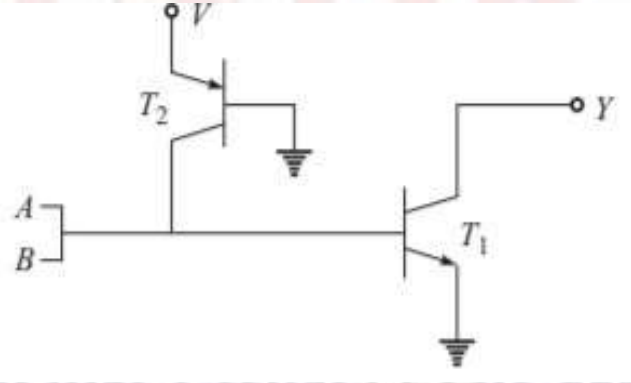
Cut-in ≈ 0.35V
(range 0.2-0.5V)





I^2L (NAND GATE)

- **When inputs A and B are low or any one of the inputs is low, the current provided by T2 is sinked by the source, T1 is OFF, and the output is high.**
- **When both the inputs are high, the base current of T1 is the sum of currents provided by the source and T2, transistor T1 is ON and the output is low.**



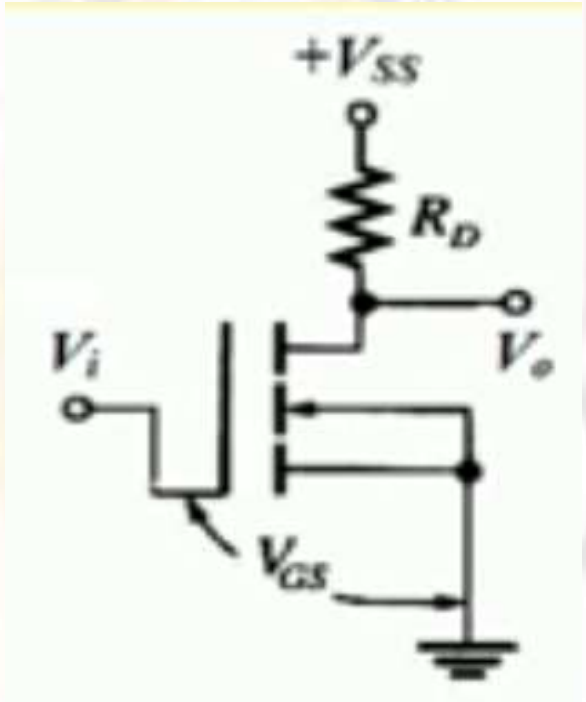
Inputs		Output
A	B	Y
0	0	1
0	1	1
1	1	1
1	1	0

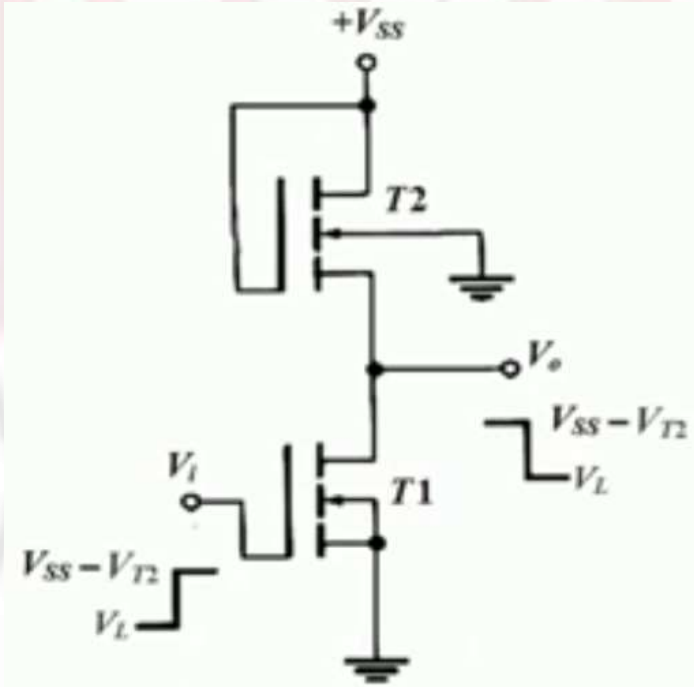
Digital Logic Families

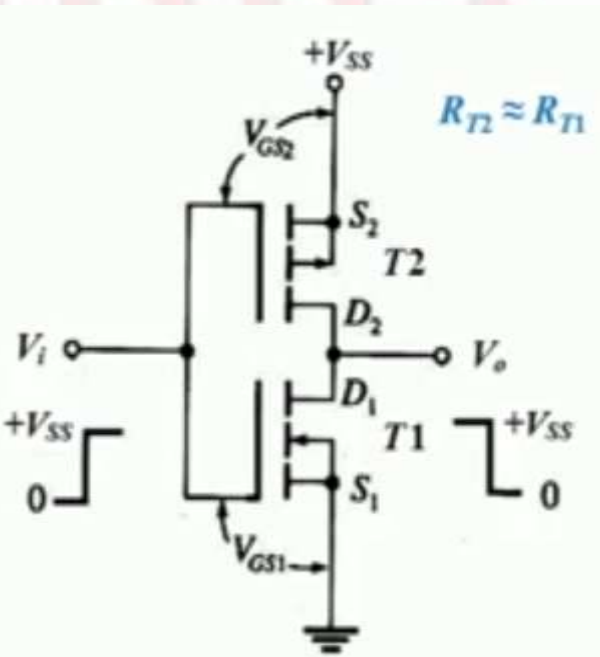
- Digital integrated circuits are classified not only by their complexity or logical operation, but also by the specific circuit technology to which they belong. The circuit technology is referred to as a *digital logic family*.
- Each logic family has its own basic electronic circuit upon which more complex digital circuits and components are developed. The basic circuit in each technology is a NAND, NOR, or inverter gate. The electronic components employed in the construction of the basic circuit are usually used to name the technology. Many different logic families of digital integrated circuits have been introduced commercially. The following are the most popular:
- TTL transistor–transistor logic;
- ECL emitter-coupled logic;
- MOS metal-oxide semiconductor;
- CMOS complementary metal-oxide semiconductor

CMOS complementary metal-oxide semiconductor

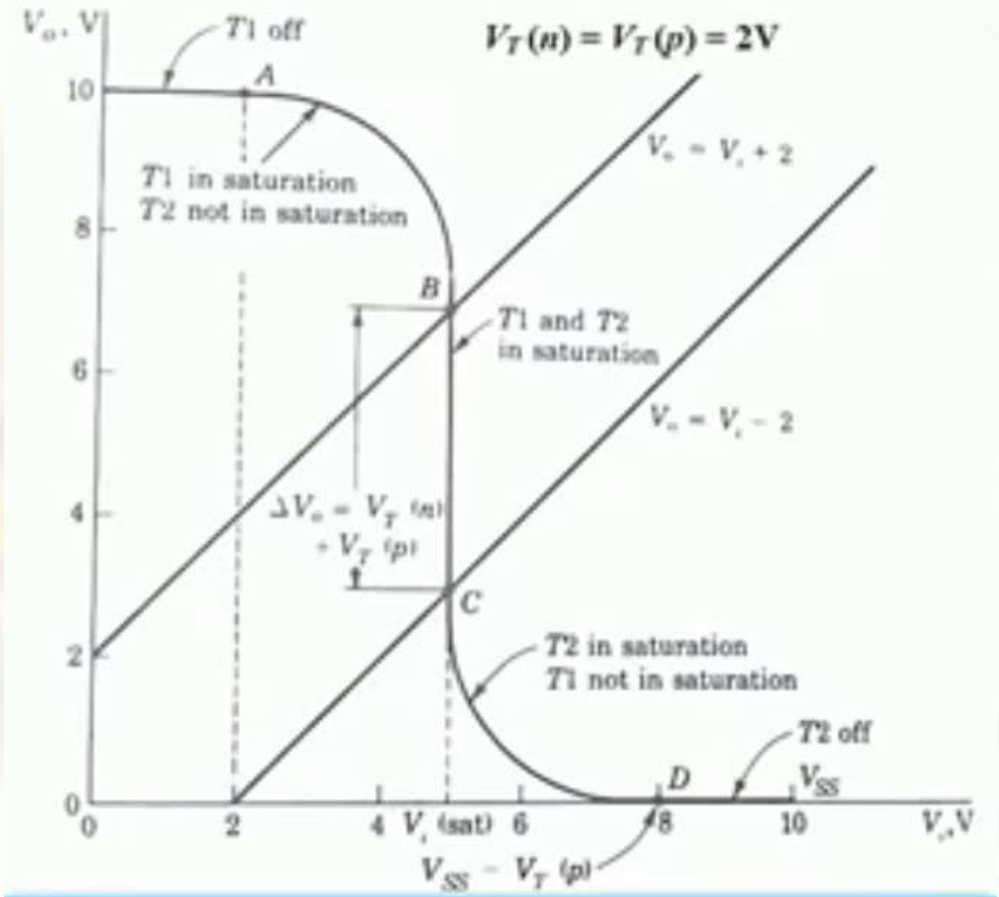
Inverter circuit







CMOS Transfer Characteristics



- $V_i \le V_T(n)$: T_1 OFF, T_2 ON, $V_o < V_{SS} \Rightarrow V_i \le 2V$
- $V_i \ge V_{SS} - V_T(n)$: T_2 OFF, T_1 ON, $V_o = 0V \Rightarrow V_i \ge 8V$
- T_1 saturated: $V_{DS1} \ge V_{GS1} - V_T(n)$

  i.e. $V_T(n) \le V_i \le V_o + V_T(n) \Rightarrow V_o \ge V_i - 2$

T_2 saturated: $V_{SD2} \ge V_{SG2} - V_T(p)$

i.e. $V_o - V_T(p) \le V_i \le V_{SS} - V_T(p) \Rightarrow V_o \le V_i + 2$

Simultaneous saturation at unique $V_{i(sat.)}$

$$V_{i(sat.)} = 5V \text{ for } k_p = k_n$$

CMOS Transfer Characteristics

★ Region-1

★ In this region the input is in the range of (0,Vtn). Since the input voltage is less than Vtn, the NMOS is in **cutoff region.** No current flows from Vdd to Vss, The entire Vdd will appear at the Output terminal.

- NMOS is in cutoff as Vgs < Vtn
- PMOS is in **linear** as Vgsp < Vtp and Vdsp > Vgsp -Vtp.
- Zero current flows from supply voltage and the power dissipation is zero.

★ Region-2

★ In this region the input is in the range of (Vtn,Vdd/2). Since the input voltage is greater than Vtn the NMOS is conducting and it jumps to saturation as it has large Vds across it (Vout is high). PMOS still remains in the linear region.

- NMOS is in **saturation** as Vgs > Vtn and Vout >Vin - Vtn.
- PMOS is in **linear** region as Vdsp > Vgsp -Vtp.
- since both the transistors are conducting some amount of current flows from supply in this region.

★ Region-3

★ In this region the input voltage is Vdd/2. At this point the output voltage is also Vdd/2 as one can see in figure-2. At this voltage both the NMOS and PMOS are in saturation and the output drops drastically from Vdd to Vdd/2. At this point a large amount of current flows from the supply. Most of the power consumed in CMOS inverter is at this point. So care should be taken that the Input should not stay at Vdd/2 for more amount of time.

- NMOS is in **saturation** as Vgs > Vtn and Vout >Vin - Vtn.
- PMOS is in **saturation** as Vgsp < Vtp and Vdsp < Vgsp -Vtp.
- Large amount of current is drawn from supply and hence large power dissipation.

CMOS Transfer Characteristics

★ Region-4

★ In this region the input voltage is in the range of (Vdd/2 , Vdd-Vtp). Here the PMOS remains in saturation as Vout < Vin - Vtp and Vgsp < Vtp. But the NMOS moves from saturation to linear region since the drain to source voltage now is less than Vgsn-Vtn.

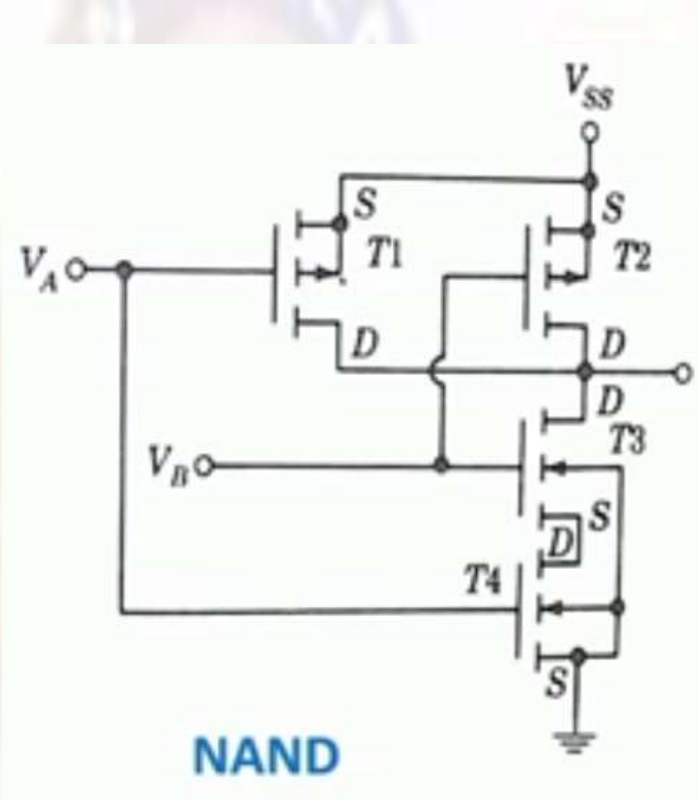
- NMOS is in **linear** as Vgs > Vtn and Vout < Vin - Vtn.
- PMOS is in **saturation** as Vgsp < Vtp and Vdsp < Vgsp -Vtp.
- A medium amount of current is drawn as NMOS is in linear region and power dissipation is low.

★ Region-5

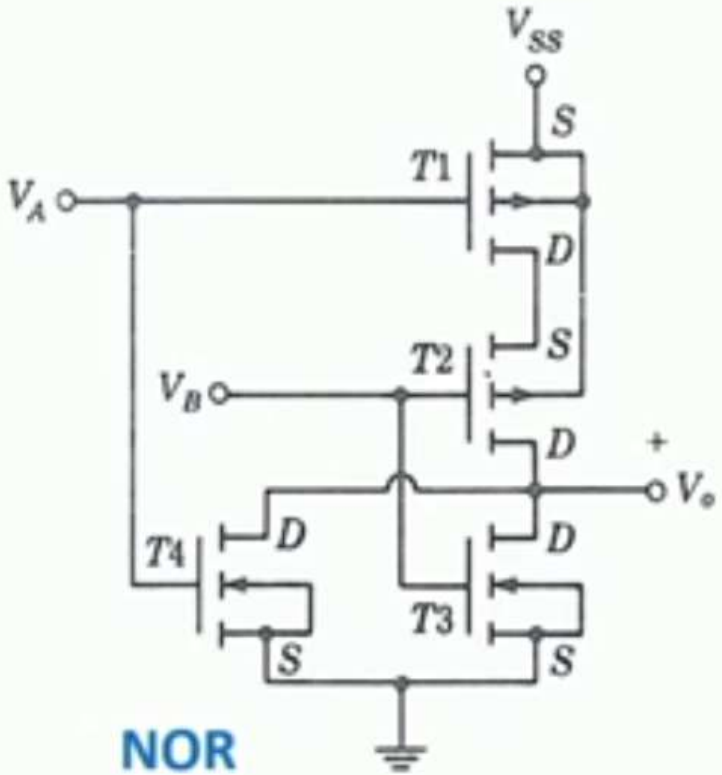
★ In this region the input voltage is in the range of (Vdd-Vtp,Vdd). Here the PMOS moves from saturation to cutoff as the Vgsp is so high that Vgsp > Vtp. The NMOS still remains in linear as the drain to source voltage now is less than Vgsn-Vtn.

- NMOS is in **linear** as Vgs > Vtn and Vout < Vin - Vtn.
- PMOS is in **cutoff** as Vgsp > Vtp.
- Zero current flows from the supply and so the power dissipation is zero.

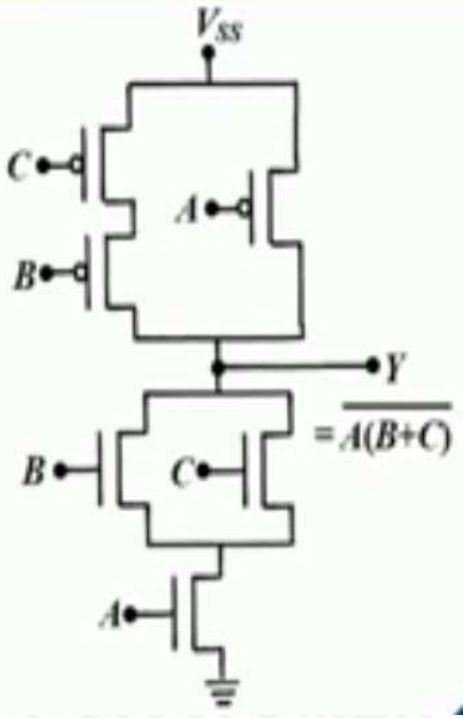
CMOS Combinational Circuits



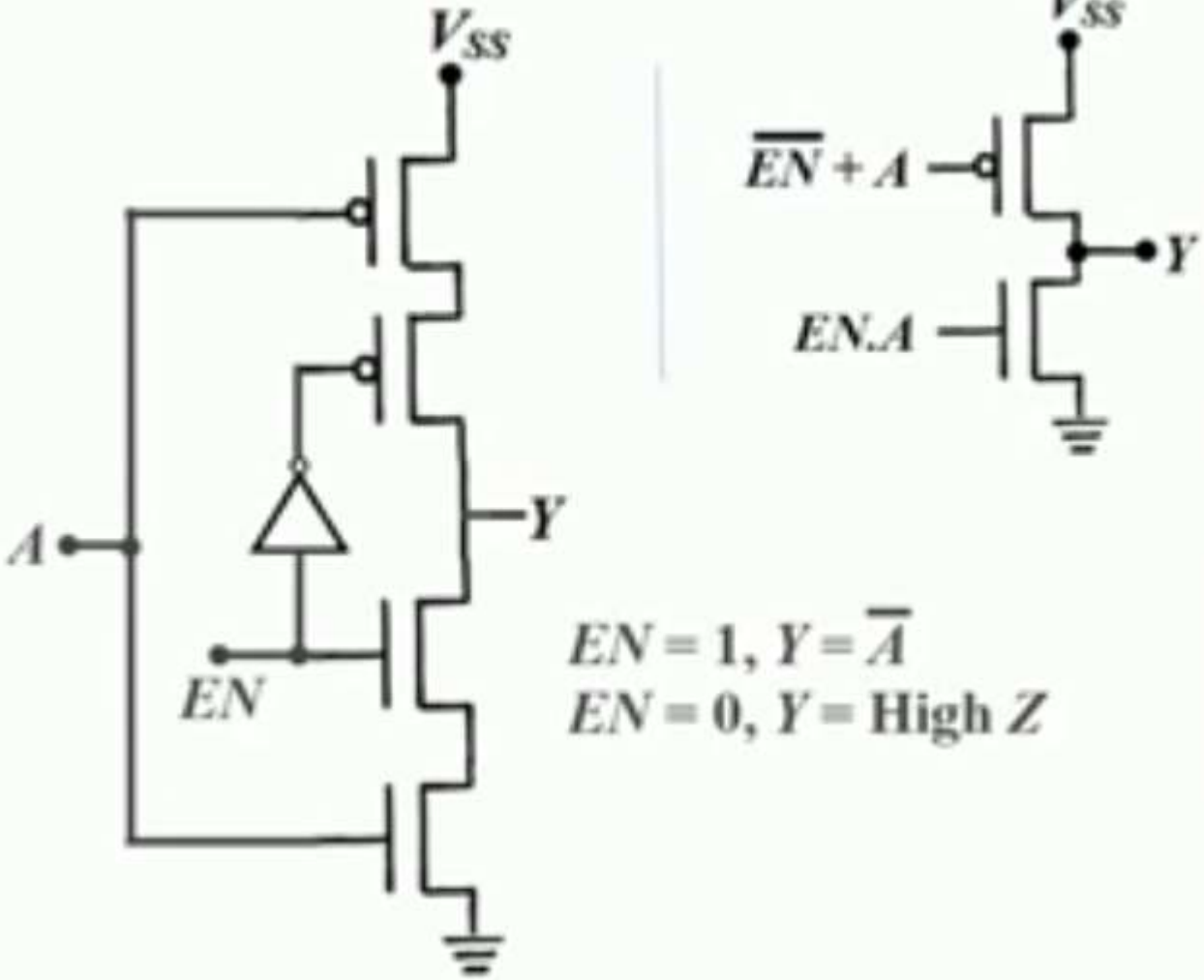
NAND



NOR



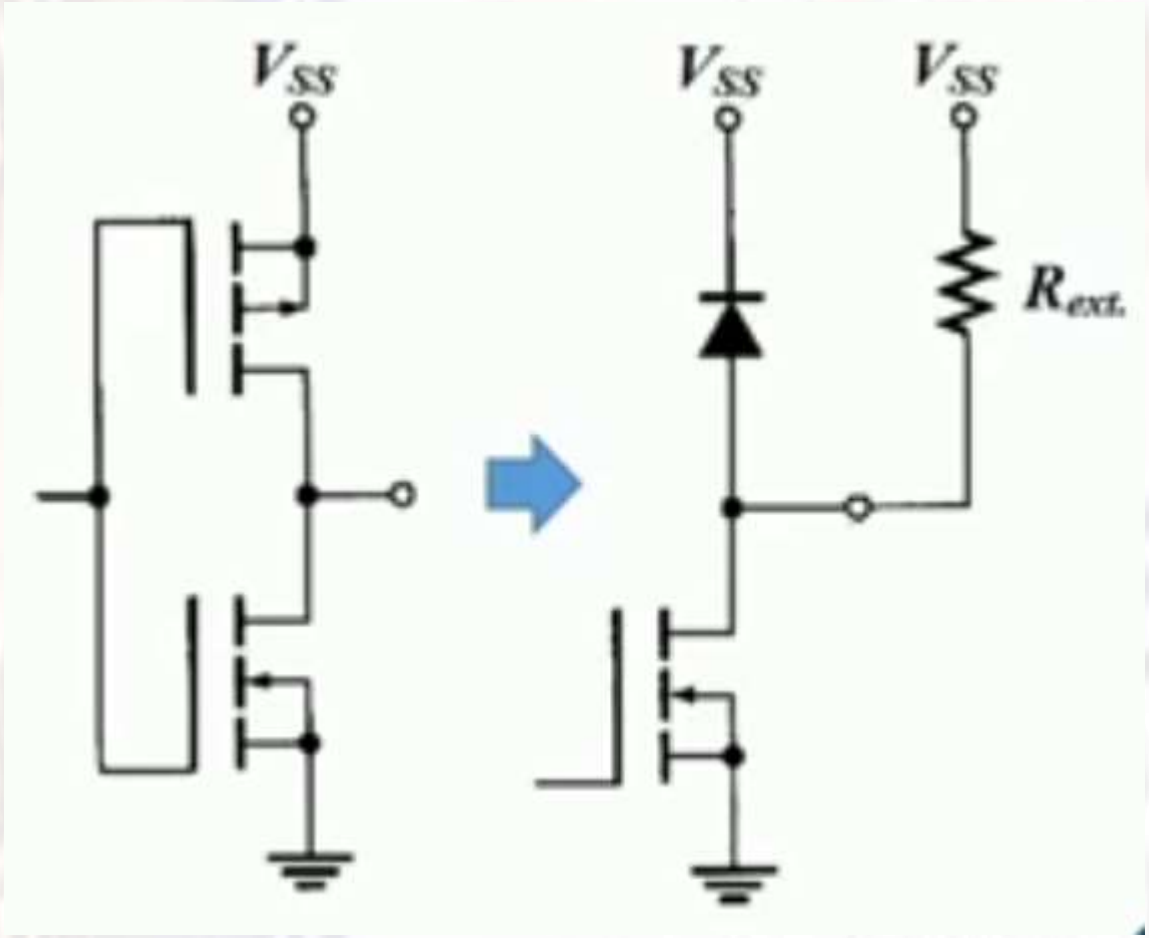
CMOS Tristate Logic



$EN = 1, Y = \overline{A}$

$EN = 0, Y =$ High Z

CMOS Open Drain logic



CMOS and TTL interface

Both: 5V Supply

Parameter	CMOS	TTL	Unit
V_{IH}	3.5	2	V
V_{IL}	1.5	0.8	V
I_{OH}	-0.5	-0.4	mA
I_{OL}	0.4	16	mA
V_{OH}	4.99	2.4	V
V_{OL}	0.01	0.4	V
I_{IH}	10^{-6}	40	μA
I_{IL}	-10^{-6}	-1.6	mA

TTL driving CMOS

- No issue with current levels.
- Issue with $V_{OH(TTL)} < V_{IH(CMOS)}$
- Pull-up resistance (2 - 6 kΩ) used

CMOS driving TTL

- No issue with voltage levels.
- Issue with $|I_{OL(CMOS)}| < |I_{IL(TTL)}|$
- CMOS buffer used
  - dimension increased, ≈ 4mA

Hamming Code

- One of the most common error-correcting codes used in RAMs was devised by R. W. Hamming. In the Hamming code, *k* parity bits are added to an *n* -bit data word, forming a new word of *n* + *k* bits. The bit positions are numbered in sequence from 1 to *n* + *k*. Those positions numbered as a power of 2 are reserved for the parity bits. The remaining bits are the data bits. The code can be used with words of any length.
- Consider, for example, the 8-bit data word 11000100. We include 4 parity bits with

Bit position:	1	2	3	4	5	6	7	8	9	10	11	12
	P_1	P_2	1	P_4	1	0	0	P_8	0	1	0	0

The 4 parity bits, P_1, P_2, P_4, and P_8, are in positions 1, 2, 4, and 8, respectively. The 8 bits of the data word are in the remaining positions. Each parity bit is calculated as follows:

$$P_1 = \text{XOR of bits } (3, 5, 7, 9, 11) = 1 \oplus 1 \oplus 0 \oplus 0 \oplus 0 = 0$$

$$P_2 = \text{XOR of bits } (3, 5, 7, 10, 11) = 1 \oplus 0 \oplus 0 \oplus 1 \oplus 0 = 0$$

$$P_4 = \text{XOR of bits } (5, 6, 7, 12) = 1 \oplus 0 \oplus 0 \oplus 0 = 1$$

$$P_8 = \text{XOR of bits } (9, 10, 11, 12) = 0 \oplus 1 \oplus 0 \oplus 0 = 1$$

Hamming Code

- Remember that the exclusive-OR operation performs the odd function: It is equal to 1 for an odd number of 1's in the variables and to 0 for an even number of 1's. Thus, **each parity bit is set so that the total number of 1's in the checked positions, including the parity bit, is always even.**
- The 8-bit data word is stored in memory together with the 4 parity bits as a 12-bit composite word. Substituting the 4 *P* bits in their proper positions, we obtain the 12-bit composite word stored in memory:

	0	0	1	1	1	0	0	1	0	1	0	0
Bit position:	1	2	3	4	5	6	7	8	9	10	11	12

When the 12 bits are read from memory, they are checked again for errors. The parity is checked over the same combination of bits, including the parity bit. The 4 check bits are evaluated as follows:

$$C_1 = \text{XOR of bits } (1, 3, 5, 7, 9, 11)$$

$$C_2 = \text{XOR of bits } (2, 3, 6, 7, 10, 11)$$

$$C_4 = \text{XOR of bits } (4, 5, 6, 7, 12)$$

$$C_8 = \text{XOR of bits } (8, 9, 10, 11, 12)$$

★ A 0 check bit designates even parity over the checked bits and a 1 designates odd parity. Since the bits were stored with even parity, the result, $C = C8C4C2C1 = 0000$, indicates that no error has occurred. However, if C 0, then the 4-bit binary number formed by the check bits gives the position of the erroneous bit. For

Bit position:	1	2	3	4	5	6	7	8	9	10	11	12	
	0	0	1	1	1	0	0	1	0	1	0	0	No error
	1	0	1	1	1	0	0	1	0	1	0	0	Error in bit 1
	0	0	1	1	0	0	0	1	0	1	0	0	Error in bit 5

In the first case, there is no error in the 12-bit word. In the second case, there is an error in bit position number 1 because it changed from 0 to 1. The third case shows an error in bit position 5, with a change from 1 to 0. Evaluating the XOR of the corresponding bits, we determine the 4 check bits to be as follows:

	C_8	C_4	C_2	C_1
For no error:	0	0	0	0
With error in bit 1:	0	0	0	1
With error in bit 5:	0	1	0	1

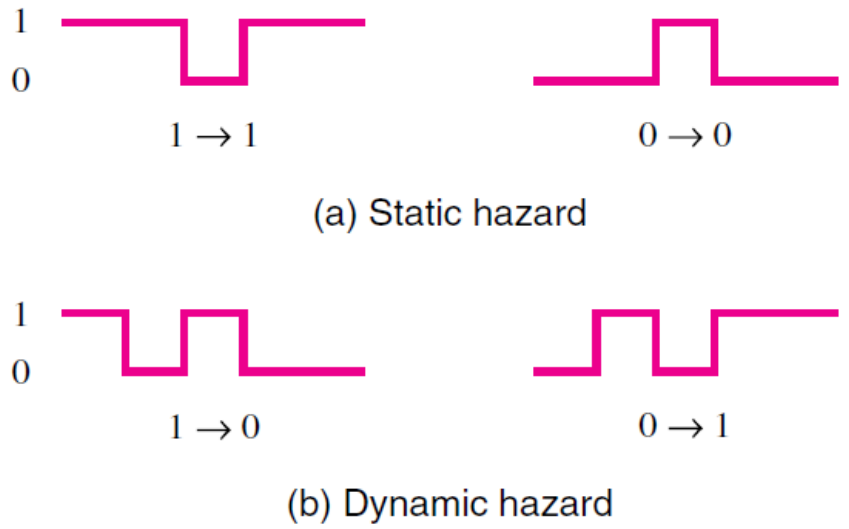
Thus, for no error, we have $C = 0000$; with an error in bit 1, we obtain $C = 0001$; and with an error in bit 5, we get $C = 0101$. When the binary number C is not equal to 0000, it gives the position of the bit in error. The error can be corrected by complementing the corresponding bit. Note that an error can occur in the data word or in one of the parity

Hazards

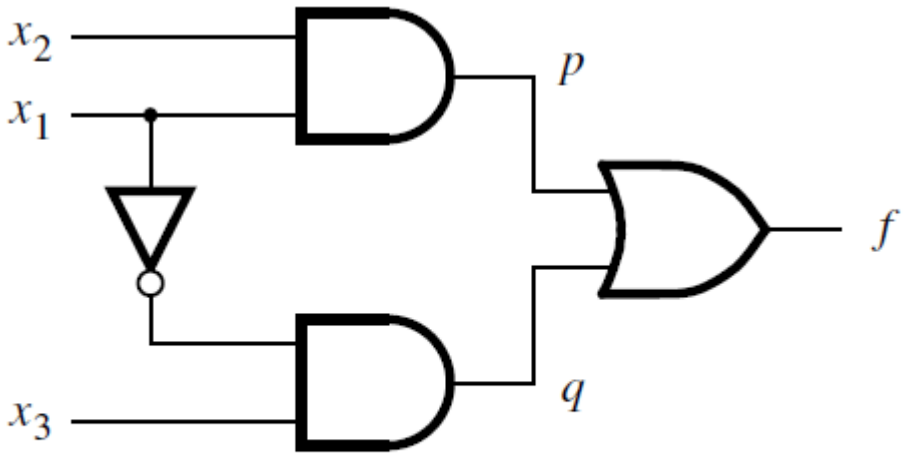
★ In asynchronous sequential circuits it is important that undesirable glitches on signals should not occur. The designer must be aware of the possible sources of glitches and ensure that the transitions in a circuit will be glitch free. The glitches caused by the structure of a given circuit and propagation delays in the circuit are referred to as *hazards*.

A *static hazard* exists if a signal is supposed to remain at a particular logic value when an input variable changes its value, but instead the signal undergoes a momentary change in its required value. One type of static hazard is when the signal at level 1 is supposed to remain at 1 but dips to 0 for a short time. Another type is when the signal is supposed to remain at level 0 but rises momentarily to 1, thus producing a glitch.

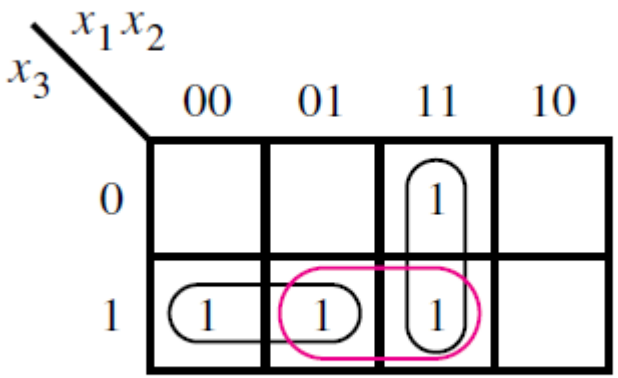
A different type of hazard may occur when a signal is supposed to change from 1 to 0 or from 0 to 1. If such a change involves a short oscillation before the signal settles into its new level, then a *dynamic hazard* is said to exist.



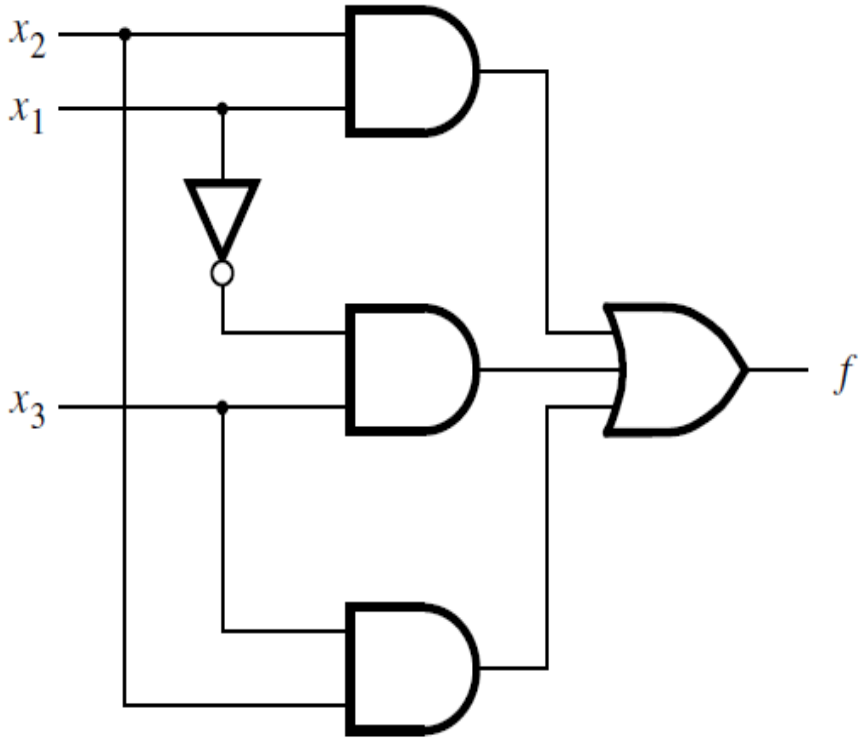
Example for Hazards



(a) Circuit with a hazard



(b) Karnaugh map



(c) Hazard-free circuit

Direct Coupled Transistor Logic(DCTL)

★ In direct coupled transistor logic, the input signal is directly given to the base of the transistor. In DCTL, the transistor operates in saturation or cut-off region.
★ The operation of DCTL is same as the operation of RTL.

- When both the inputs are in logic 0, transistors operate in cut-off, and the output is logic 1.
- When any one of the inputs or both the inputs are in logic 1, the corresponding transistor or transistors operate in saturation and the output is logic 0.
- Although DCTL is simpler than RTL, it is not popular because of the current hogging problem